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Volume III

ADVANCED INERTIAL TECHNOLOGIES

Volume III

The Charles Stark Draper Laboratory, Inc.

June 1975

TECHNICAL REPORT AFAL-TR-73-124, VOLUME III

Final Report for Period 1 July 1974 through 15 February 1975

Air Force Avionics Laboratory
Air Force Systems Command
Wright-Patterson Air Force Base, Ohio 45433

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This report has been reviewed and is approved for publication.

MARVIN SPECTOR, Acting Chief
Navigation and Weapon Control Branch

FOR THE COMMANDER

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Gyro Spin-Axis Gas Bearings	Porous Polyimide Retainer Material
Gyro Spin-Axis Ball Bearings	Hypha Interpolator
Activated Reactive Evaporation	Digital Phase-Locked Loop
Hard-Surface-Material Coatings	Hypha Heterodyner

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes the final part of an exploratory development program of study, design, fabrication, and test of advanced inertial-sensing instrument technology. Activities covered include: (1) spin-axis gas- and ball-bearing advances through improved deposition techniques and ball-retainer material, (2) continuation of the investigation of hybrid-phase (Hypha) signal-processing and conversion techniques, (3) continuation of the investigation of motion compensation of advanced radar, and

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Modified Hypha Dynamic Navstar Frequency Synthesizer
Hypha Universal Servo
Electronics-Instrument-Servo-Technology Investigation
Motion Compensation
Synthetic-Aperture Radar
Inertial Components
Master/Slave Studies

20. ABSTRACT (Cont.)

(4) continuation of support for the Electronically Agile Radar (EAR) Program Office at AFAL.

FOREWORD

This report, AFAL-TR-73-124, Volume III (Charles Stark Draper Laboratory Report R-859) was prepared under Project 6095 Task 02, covering the period 1 July 1974 through 15 February 1975, through Air Force Contract F33615-72-C-1335 by The Charles Stark Draper Laboratory, Inc. Cambridge, Massachusetts 02139.

The monitoring Air Force Project Engineer is Capt. Edwin V. Harrington, Jr. AFAL/RWN, Air Force Avionics Laboratory, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio 45433. This report was submitted by the author in March 1975.

This report contains no classified material.

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ADVANCED INERTIAL TECHNOLOGIES

INTRODUCTION

This is the third and final installment of the R&D technical report covering work under contract F33615-72-C-1335 from 1 July 1974 through the end of the contract on 15 February 1975. The report is submitted in fulfillment of item A003 of the CDRL dated 8 October 1971.

In accordance with the Statement of Work, the overall objective was to conduct an exploratory development program of study, design, fabrication, and test of advanced inertial-sensing-instrument technology and other navigation-system technology, and to consider and recommend applications for the technology developed. To accomplish this goal, the program was broken down into the following tasks and subtasks:

Task 1—Gyro-Technology Development

This effort was subdivided into three tasks with overall goals being to improve gyro spin-axis bearing technology, aimed at improving reliability, performance, and cost, and to provide assistance to G200-gyro spin-axis-bearing vendors to ensure that the product meets its specifications.

Task 1.1—Gas-Bearing-Technology Effort

The gas-bearing-technology effort has its emphasis on developing hard-surface-material coatings with high-rate coating techniques directed toward spin-axis gas-bearing application.

Task 1.2—Ball-Bearing-Technology Effort

The ball-bearing-technology effort has its emphasis on improvements to the ball retainer material in the areas of pore-size distribution, pore volume, and consideration of a lubricant filler material.

Task 1.2.1—On-Site Assistance on G200 Program

Effort under this task was concluded at the end of the previous reporting period.

Task 2—System-Technology Development

This task was divided into three major subtasks.

Task 2.1—Electronic-Instrument-Servo-Technology Investigation

Hybrid-Phase (Hypha) technology has many applications such as in navigation receiver systems, data acquisition systems, and various types of servo-control systems.

CSDL has developed a DPLL (Digital Phase-Locked Loop) and has applied for two patents which are awaiting action in the U.S. Patents Office. This design, which is expected to be a useful system building block in navigation receiver systems, is now being made into an integrated circuit.

A modified Hypha Heterodyner technique is being utilized to develop a Dynamic Navstar Frequency Synthesizer. A short discussion of the Navstar System is presented as a means of defining the requirements for such a synthesizer and as a means of justifying CSDL's design approach to the problem. In addition, a block-diagram circuit description is presented of the entire concept.

Hypha technology has already been shown in earlier studies to be applicable to A/D conversion. As an extension of these studies, a Hypha Resolver-to-Digital Converter (R/D) has been built and tested. Linearity and accuracy results are published in the report. They show that this technology is comparable to other existing techniques in this area.

In order to reduce the quantization errors in pulse rebalance instruments, Hypha technology in the form of an interpolator has proved to be an effective tool. The interpolator is shown to provide high-frequency filtering of noise while preserving low-frequency information. In addition an extension of this technology imbeds similar circuitry within the control loop of a servo-type system. It is hoped that Hypha designs will lend themselves to developing a very flexible servo-loop building block.

Task 2.2—Motion Compensation of Advanced Radar

The overall objective of this investigation was to identify what existing motion-sensor instrumentation or combination of available sensors having a mature production base could be used to accomplish motion compensation for the Electronically Agile Radar (EAR).

Task 2.3—Integrated Digital Avionics

Effort under this task was concluded at the end of the previous reporting period.

Task 3—Technology Transfer

The goal of this task is to disseminate the technology developed under this and other Air Force contracts to other government agencies and to industry as directed. Since this is an ongoing program carried out under all of the technical tasks by means of publication of reports, presentation of papers, attendance at symposia, etc., this task is not reported on separately in this report.

Task 4—EAR Antenna Mounted Motion-Compensation Investigation

CSDL provided engineering support to the Electronically Agile Radar (EAR) Program Office during the period of performance of this contract.

This report is broken down into four major parts, each one covering activities under one of the major tasks or subtasks actively being pursued during this reporting period, as follows:

Part A	Task 1—Gyro Technology Development
Part B	Task 2.1—Electronics-Instrument-Servo-Technology Investigation
Part C	Task 2.2—Motion Compensation of Advanced Radar
Part D	Task 4—EAR Antenna Mounted Motion-Compensation Investigation

For ease of reference, the light blue sheets signify the start of each new part.

PART A

GYRO-TECHNOLOGY INVESTIGATION

Section 1—Gas-Bearing Technology by K. A. Taylor

Section 2—Ball-Bearing Technology by P. R. Kerrigan

SECTION 1

GAS-BEARING TECHNOLOGY

1.1 Introduction

Activity in the development of spin-axis gas-bearing technology continues to be combined in the development of high-rate coating techniques for the application of thick film coatings for gas-bearing surfaces. The configuration of primary interest is the opposed-hemisphere hydrodynamic gas-bearing assembly with grooves on the stationary inner-bearing part. Homogeneous coatings applied by high-rate-deposition techniques are being developed as a replacement for the more porous melt-spray deposits presently in use. The high-rate-deposition process combines sputtering and electron-beam evaporation techniques to produce coatings 0.001 to 0.010 inch in thickness, as required. A system capable of applying these coatings to lightweight thermally conductive substrates such as beryllium was developed in prior reporting periods, and has been modified during this period to accomplish the more complex processing shown to be necessary to form the coatings uniformly about shaped substrates.

Efforts directed toward the sputter deposition of cermet-type materials within this reporting period have been limited to producing samples for coatings having a tungsten-carbide/cobalt matrix by conventional sputtering for wear testing in the University of Rhode Island's (URI) wear tester.

1.2 Sputter Deposition

A coating of tungsten carbide with cobalt was selected for initial attempts at sputter deposition by conventional RF sputter techniques. This choice was indicated by past experience on other programs showing that solid spherical inner-bearing parts manufactured from Carbolloy 44A (WC + 6% Co) gave a high level of bearing life when used with outer-bearing parts made from aluminum oxide (Al_2O_3). Two beryllium discs (one inch dia.) were coated and an interfacial layer of titanium was provided

on one of the discs to increase adhesion. The beryllium surfaces were lapped to a high polish prior to coating, and polished again very lightly after coating to remove any dendrite growths in the coating. Figure 1-1 shows these specimens after wear testing.

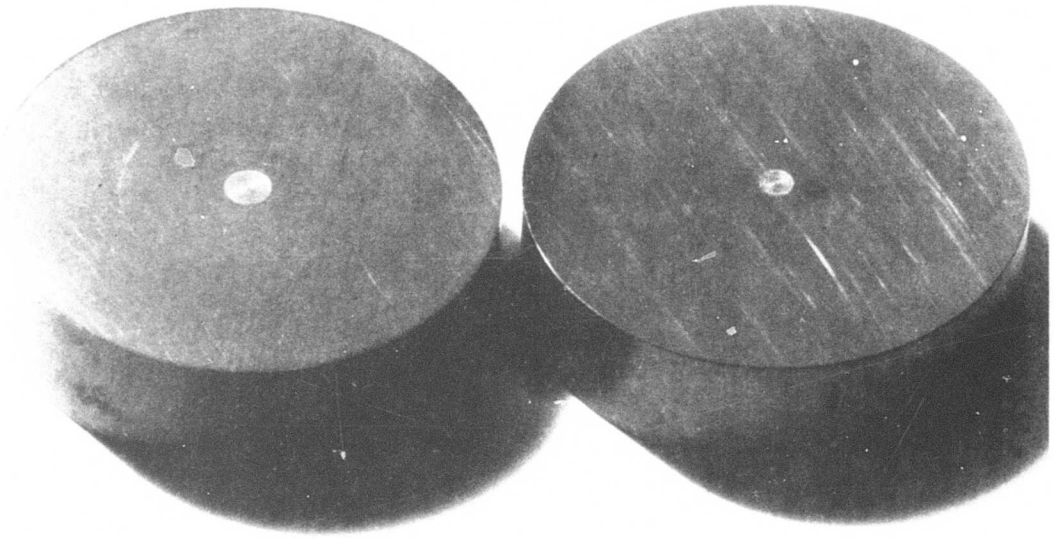

Figure 1-1. Specimen pair coated on upper face with a sputter-deposited tungsten-carbide and cobalt coating. (The center region of the specimen as shown is depressed and not part of the wear surface.)

These specimens were installed in the URI wear tester and subjected to the conditions given in Table 1-1.

Table 1-1. Wear-tester run conditions.

Run No.	1	2
Time	11 min	10 min
Load	250 gm	700 gm
Speed	500 r/min	500 r/min
Atmosphere	helium	helium

The specimens were examined at the end of Run 1. No evidence of wear or debris was observed, and the specimens were reinstalled and subjected to the parameters of Run 2. Examination at the conclusion of the test revealed a slight wear track on the stationary member. This was also the member that did not receive the titanium interface. The rotating member with the titanium interface shows no evidence of wear.

These results show considerable promise for sputter-deposited carbide coatings in gyroscope applications. Other carbide coatings to be investigated include titanium carbide and chrome carbide, both with and without nickel binders. Fixturing is also in process to transfer this coating to shaped spherical bearing parts.

1.3 High-Rate Deposition

The major effort for this period was directed toward the further development of the activated reactive evaporation (ARE) for titanium-carbide deposition. 100-percent titanium carbide of sufficient thickness to satisfy surface finish and dimensional requirements has been shown by wear testing to withstand periods of sustained rubbing under load with no evidence of wear debris or change in the coefficient of friction. This process was originally developed by Professor R. F. Bunshah of the Materials Department of the University of California at Los Angeles and has been shown to produce consistently hard titanium-carbide coatings on flat beryllium substrates. Gas scattering, a modification of the ARE process, is intended as a means of coating spherical bearing parts. It has been demonstrated that a uniform coating can be applied over a spherical surface using this technique; however, exact definition of the many parameters which affect the coating has not yet been attained.

Other materials that were tried briefly were titanium diboride and titanium nitride. Titanium diboride is of interest because its mechanical properties suggest that it would be a suitable bearing material, and it can be evaporated by electron-beam techniques without requiring a chemical reaction. Titanium nitride is also a hard material that can be formed by reactive evaporation and does not produce the process-inhibiting byproducts that result from carbide depositions.

1.3.1 Facility

The high-rate coating facility was found to have inadequate pumping speed to allow coatings at the high pressures necessary to produce gas scattering for the coverage of shaped parts, and still allow the operation of the electron-beam gun. Coatings by gas scattering are accomplished at chamber pressures greater than 2×10^{-2} torr in contrast to the electron-beam gun which requires pressure less than 5×10^{-4} torr. High pumping speed is also necessary to remove the by-products of the titanium-acetylene reaction, notably hydrogen and methane. Failure to remove or prevent the build-up of high concentrations of these gases will result in soft titanium-rich coatings.

A 10-inch high-speed diffusion pump was purchased from CVC Vacuum Products of Rochester, New York and installed in place of the original 6-inch diffusion pump. A custom high-conductance valve assembly was fabricated and installed at International Vacuum, Inc. of Pembroke, Massachusetts. This change resulted in a pumping speed of approximately 3000 liters per second at the electron-beam-gun filament. Adequate pressure differentials were obtained. Byproduct removal was enhanced by the addition of the original 6-inch pump to the upper region of the chamber where coating takes place. This change resulted in approximately 1500 liters per second of pumping speed available for control of the coating atmosphere. The system is shown schematically in Figure 1-2.

1.3.2 Titanium-Carbide Coating

Titanium carbide, as deposited by high-rate-deposition techniques, normally results in a coating that is extremely hard and fully dense. Results in this reporting period showed that hardnesses in the range of KHN_{500} 1600-2200 could be repeatedly produced on flat substrates within the accuracy range of the measuring equipment. It was also observed, with a series of calibration runs that, as the titanium was depleted, the evaporation rate increased from 1.5 grams per minute to 2.0 grams per minute, and that the deposition rate increased accordingly. The average deposition was observed to be approximately 0.2 mils per minute.

The work of others has shown that the biasing that provides the activation by ionizing the vapor can be either positive or negative. When the bias is applied to the substrate, not a separate ring, the bias-hardness relationship is as shown in Figure 1-3.

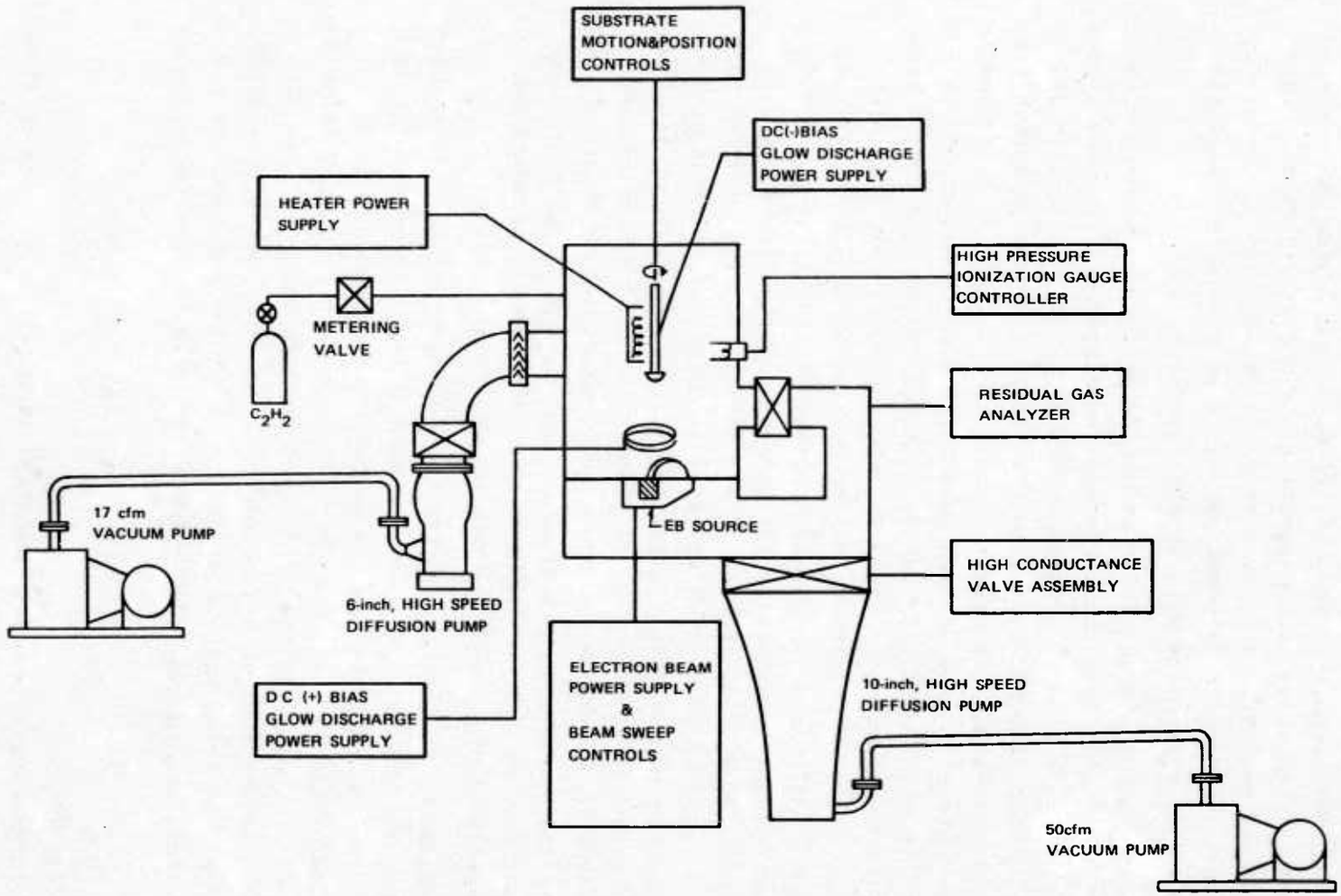

Figure 1-2. Schematic of high-rate coating system set up for activated-reactive-evaporation coatings.

This curve shows that hardness is relatively insensitive to negative bias and quite sensitive to positive bias, the region that we have been working in. Negative bias capability has been added to the high-rate coating system. Typical values of -3000 Vdc and 100 mA repeatedly produce hard titanium-carbide coatings. This is basically ion plating, and it appears to work quite well on flat surfaces.

Results reported in the prior reporting period showed that rotating the substrate in order to uniformly coat a spherical diameter was unsuccessful in that a layered structure developed. As the surface to be coated passed from line of sight with the titanium source, a carbon film developed, and produced a layered structure with poor interlayer bonding. Efforts in this period were devoted toward the development of the gas-scattering process. Spherical bearing parts coated by this method have not withstood the lapping process. Coatings of sufficient integrity and distribution to be subjected to lapping have been soft and titanium rich, due to insufficient reaction. A number of individual parts were coated in an attempt to determine the optimum coating parameters. An SEM examination of a cross section of a sputtered coating revealed that the initially applied free-titanium layer (applied for adhesion purposes) was much thicker than expected, resulting in an outer layer of titanium carbide thinner than anticipated (see Figure 1-4). Coatings applied with increased acetylene have shown a very weak structure characterized by porosity and an excess of carbon. An analysis of the present technique is in progress. X-ray diffraction of the samples is being done to metallurgically categorize the structure more definitely.

Professor R. F. Bunshah recently recommended that both a negative bias on the substrate part and a positive bias on the glow ring be used. The purpose of the positive bias is to promote the reaction of the titanium and acetylene and the negative bias promotes the coating distribution and integrity on the surface of the substrate. It was also recommended that coating in a high pressure of acetylene, approximately 2×10^{-2} torr, be tried without argon. Both of these suggestions are presently being considered and coating runs are in process to evaluate them.

1.3.3 Wear Testing

The SAMSO program (Contract F04701-74-C-0047) to perform friction and wear analysis on gas-bearing materials was completed during this

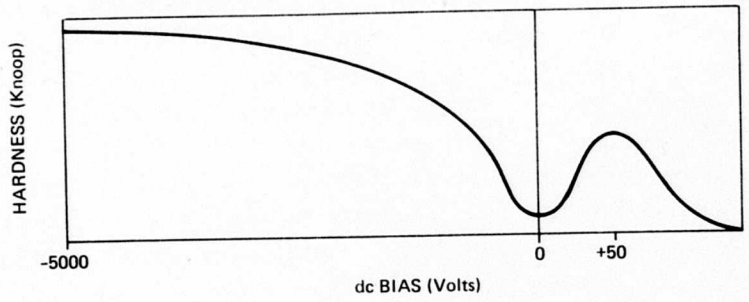

Figure 1-3. Bias-versus-hardness curve.

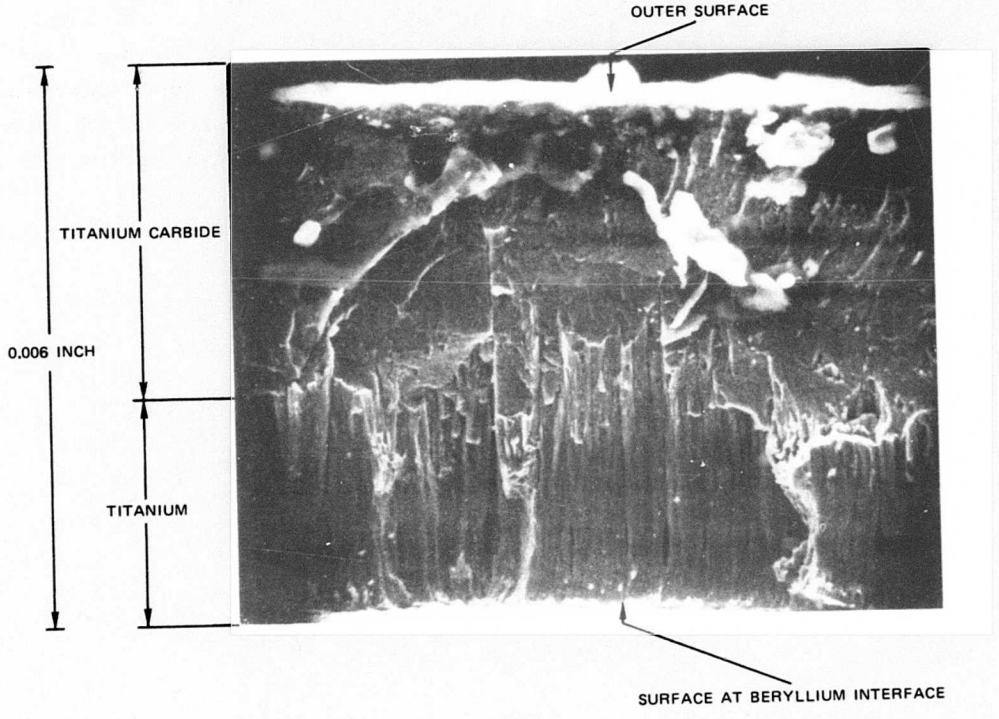

Figure 1-4. Cross-section of titanium and titanium-carbide coating from spherical inner-bearing Part 286.

reporting period. Materials considered were titanium-carbide coatings by activated reactive evaporation, chromium-oxide coatings flame deposited by Union Carbide (LC-4), solid fine-grain boron carbide, and titanium-diboride coatings applied by high-rate evaporation. It was found that no one material, as presently constituted, lived up to the ideal of a very low coefficient of friction coupled with no wear debris at any level of speed or load or environment. It was concluded that a better understanding of specific frictional characteristics and a clear knowledge of the wear mechanisms is essential.

The titanium-carbide coating showed real promise: high speeds and high loads in the helium environment produced little wear. An additional specimen pair, with one member spiral grooved by sputter etching, was tested during February 1975. The titanium-carbide coating was applied by reactive ion plating in a mixture of acetylene and argon. Acetylene was added to a pressure level to provide a hard coating on the flat surfaces and then argon was added to raise the chamber pressure sufficiently to establish a bias power level on the substrate of approximately 13.5 watts per square inch. The wear test parameters for the pair are given in Table 1-2.

Table 1-2. Wear-test parameters for ion-plated specimens.

Run No.	1	2	3
Time	10 min	10 min	10 min
Load	700 gm	700 gm	1600 gm
Speed	500 r/min	1000 r/min	1000 r/min
Atmosphere	helium	helium	helium
Friction Coefficient	0.3 to 0.5	0.13	0.11

Barely discernible marks were noted after application of the 700-gram loads, and a slight burnishing was observed after the application of the 1600-gram load. The burnished area of the grooved member is shown in Figure 1-5. Specimen diameter is one inch.

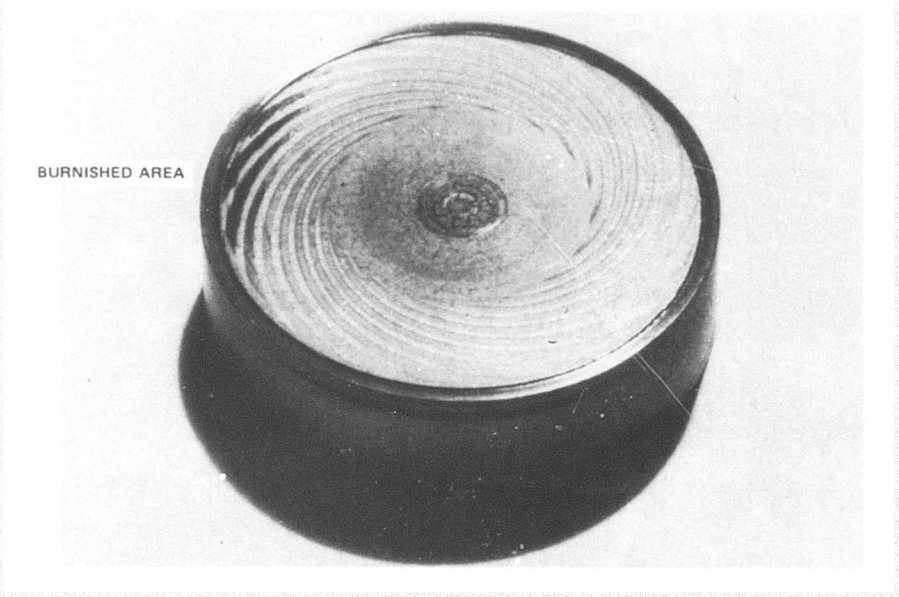

Figure 1-5. Specimen 13-2 after wear testing. Surface is coated with titanium carbide by reactive ion plating.

Results obtained from the chromium-oxide coatings indicated that a better method of surface finishing should be developed. Past results on other programs conducted at URI showed that surface stoichiometry and pretreatment significantly affect the friction and wear characteristics of oxide materials. Results showed that coefficients of friction were not as low as those observed from the other materials and appreciable amounts of debris were generated at low levels of load and speed.

Boron-carbide pairs were found to develop extensive wear debris in air in the low-energy regime. A pair of highly polished surfaces were tested in helium for a total running time of approximately 8 minutes with speed as the variable. Conditions were as given in Table 1-3. These surfaces began running very smoothly, and as they "ran-in" the coefficient decreased to values less than 0.1. After a short period of time, at low speeds and loads, the samples chattered.

Table 1-3. Boron-carbide wear-test results in a helium atmosphere.

Test No.	Speed (r/min)	Load (lb)	Coefficient of Friction
1	100	3	0.14
2	200	3	0.07
3	300	3	0.07
4	500	3	0.07

The following wear features were observed.

(1) Scratches and gouges: Associated with the wear track.

(2) Wear debris: Of extremely fine particle size (less than 1 micron). Some is free on the surface as aggregated clusters, and some is packed into a film.

(3) Holes: Present in the wear track, and appear to result from pull-outs from the surface.

This amount of wear debris was small and could not be analyzed, but it was probably boron carbide. The sudden onset of abrasive wear almost certainly was the cause of the rapid increase in the coefficient which drove the samples into the chatter condition.

The remainder of the experiments on boron carbide were performed on samples 2-0 and 4-0, and were run in air. At low speeds, considerable white-wear debris was formed on the surface, and sequences of film packing and film break-up could be followed by noise changes and coefficient changes during running. The friction values started very high, approximately at 0.9, decreasing nonlinearly; with time to a low of 0.15. The run was stopped to examine the interface, which revealed the massive white-wear debris. A subsequent run on the same surfaces from which the white debris had been removed by wiping, ran at lower coefficients. The surfaces are presumably more congruent, but eventually produced chatter.

One pair of specimens with a coating of titanium diboride was tested with less-than-optimum surface conditions. An initial coeffi-

cient of friction of 0.03 was observed and this increased to a value of 0.8 with the run ending in severe chatter after 8 minutes. The wear phenomenon was identical to that observed on titanium carbide. The overall impression on these very limited results is that titanium diboride may be promising and deserves further work on optimum surfaces.

SECTION 2

BALL-BEARING TECHNOLOGY

2.1 Introduction

This task had, as its objective, the development of an improved porous ball-retainer material. The development of a porous polyimide material by CSDL was a major step in the attainment of this goal. Designated Meldin 9000, and produced by the Dixon Corporation, it is currently in active use as the retainer material for the bearings in the G-200-gyro repair line at the Air Force AGMC.

The continuation of this effort sought to improve the polyimide material in a number of ways. The goals were:

(1) To further develop a material which would have a controllable broad pore-size range which would provide for a variety of applications.

(2) To develop alternate molding techniques which would provide a less time-consuming, thereby less-expensive, manufacturing process.

(3) To investigate the possibility of incorporating a solid lubricant into the material which would lower the friction level at the retainer/ball interface.

The task effort to the conclusion of this contract concentrated on these three areas.

2.2 Broad Pore-Size Range

A billet of material was prepared by isostatically molding Monsanto Resin 500 and Torlon. The purpose was to show broad pore-size distribution and good strength. A pair of retainers and a tensile-test specimen were prepared from the billet. The material was quite spotty in appearance due to nonuniform mixing and large particle size. The tensile specimen was tested and the tensile strength was observed to be

approximately 400 lb/in.^{2} Because of the unevenness of the mixture, it was felt the retainers would probably not perform well, so they were not assembled into a wheel.

The investigation of pore-size distributions in Torlon/Kerimid combinations was continued. These combinations had been found to form porous material with wide pore-size distributions compared to the pore-size distributions of the material obtained with other polyimides or polyamide-imides tested. Billets were prepared from a mixture of three parts Torlon and one part Kerimid that had been passed through a 75-micron sieve to produce a fine-particle size. This mixture was also passed through a 710-micron sieve producing a mixture with large-particle size. Porosimeter data showed a diffused pore-size distribution indicating intraparticle porosity (as opposed to interparticle porosity) obtained with the fine-particle size.

To investigate this further, to see if it was possible to obtain the broad-pore peak by mechanical sieving, Torlon 2000 was sieved into five fractions:

(1) Greater than 710 microns.

(2) Between 250 and 710 microns.

(3) Between 150 and 250 microns.

(4) Between 75 and 150 microns.

(5) Less than 75 microns.

and each fraction was mixed with Kerimid in a 3-to-1 mass ratio (Torlon/Kerimid). The mixture was rolled in a 16-ounce jar with 100 half-inch ceramic balls for 4 hours. Each mixture was molded isostatically and the pore-size distribution of the rod so prepared determined (rod designation INS-13-803). The results of this test showed that the coarsest fraction had the highest porosity. A large percentage of the pore volume in this coarse fraction were pores less than about 0.2 micron, while only a relatively small percentage of the pore volume were large pores, greater than 1 micron. The finest fraction of powder showed a substantially lower porosity with the majority of its pores greater than about 1 micron. Only a small percentage of the pores of the rod prepared from the fine fraction consisted of pores smaller than 0.2 micron (see Figure 2-1).

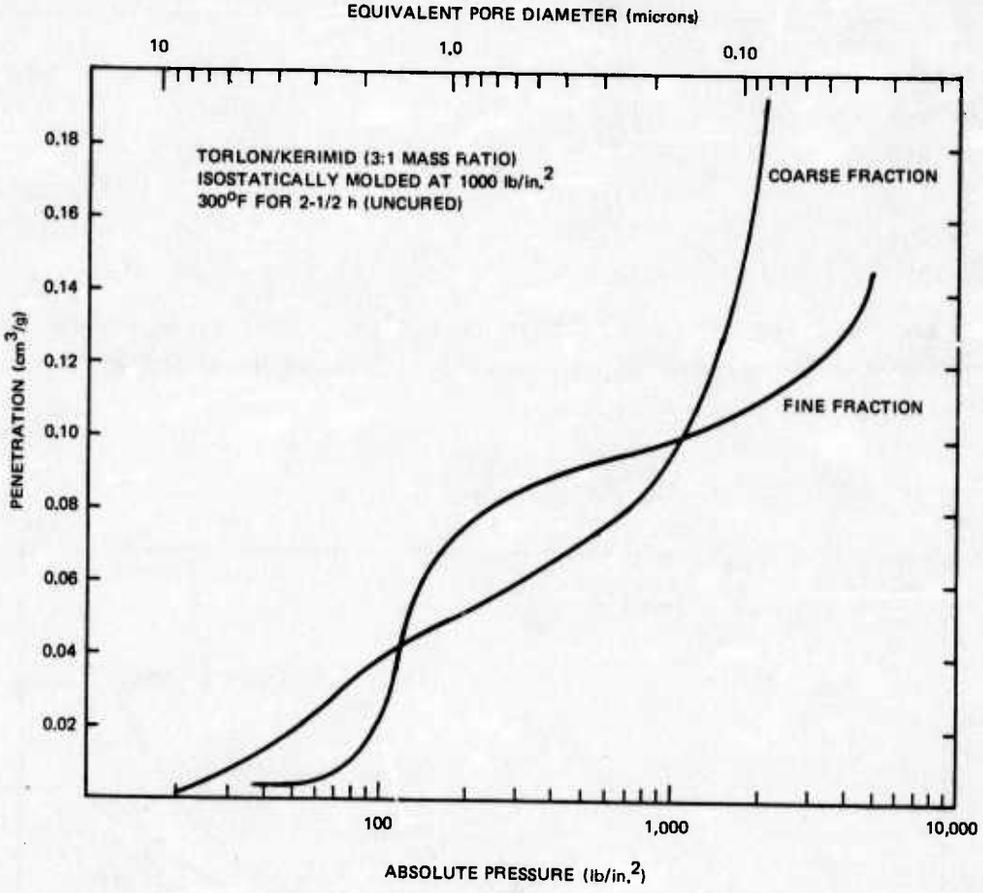

Figure 2-1. Torlon/Kerimid coarse- and fine-mixture pore-size distribution.

An additional powder mixture was prepared by reconstituting the original powder. This was done by remixing the five powders in their original proportions. The results of these tests are shown in Figure 2-2. As expected, the coarse material exhibited a wide pore-size distribution covering the intermediate- and fine-pore ranges but showed little porosity in the large pore-size range. The finer powders showed a relatively narrow distribution with the majority of the pores falling in the large and in the fine pore-size ranges. Because of the low porosities of these samples, these results did not yield as much information as had been hoped for. To provide further insight, independent density measurements on the five billets described in Figure 2-2 indicated the following values as the upper limit of the pore-size-distribution curves.

Sample No.	Penetration Benzene (cm^3/gm)	Maximum Penetration Mercury (cm^3/gm)
INS-13-786A	0.24	0.09
INS-13-786B	0.12	0.05
INS-13-786C	0.17	0.04
INS-13-786D	0.18	0.04
INS-13-786E	0.11	0.04
INS-13-787	0.11	0.06

These data indicate that there is a significant pore volume that is not detected by the mercury porosimeter, but is detected by benzene penetration in the density tests.

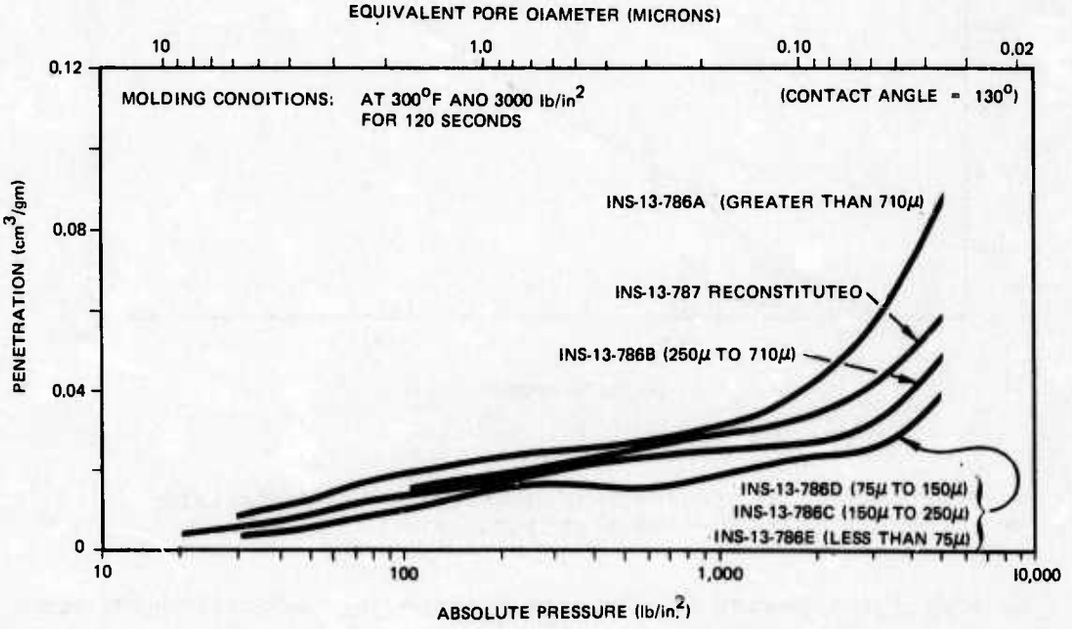

Figure 2-2. Pore-size distribution of compression-molded Torlon 2000.

2.3 Compression Molding

The second effort of this task, to develop a less-expensive manufacturing process, was approached in two ways. If the polyimide was comprised of a one-part system—as opposed to the standard two-part system of resin and binder—then the powder preparation would be greatly

simplified. Also, if the manufacturing molding process could be changed from that of an isostatic mold to a compression mold, then the retainers could have their major dimensions, OD, ID, and width, molded rather than machined. The effort in this area was a continuation of that effort described in the Interim Technical Report, AFAL-TR-73-124, Volume II.

An area of interest in considering Monsanto Resin 500 is the reduction of the particle size of the commercial powder. Control of the particle size will allow control of the pore size of the molded material prepared from the resin. A sample of Resin 500 was jet-milled (courtesy of Dixon Corp.) and another sample was hammer-milled at Monsanto, resulting in the particle-size distributions (measured by micromerograph) shown in Table 2-1.

Table 2-1. Particle-size distribution of Resin 500 under various conditions.

	As Supplied (%)	Jet-Milled (%)	Hammer-Milled (%)
Mass greater than 74	15.9	7.9	2.2
Mass greater than 44	23.2	11.5	11.1
Mass greater than 20	53.2	25.7	34.7
Mass less than 10	9.8	18.2	19.2
Median size (microns)	23.2	15.8	16.0

The difference in particle-size distribution between these various samples was not great, but it is difficult to judge the significance of these results as the extent of milling both cases was not well defined. When these powders were used to prepare compression-molded tablets, the pores of the milled materials were only slightly smaller than the pores of the resin as supplied. In an attempt to pursue this area further, additional samples were sent to the Trost Company for more intensive jet-milling under conditions that are better defined.

A Trost T-X Laboratory Model mill lined with polyurethane was employed for the testing. Collection of the product was made via a stainless steel cyclone with the air filtered through a Dacron air-relief bag.

In the first three tests there was difficulty in reducing the particle size (see Table 2-2). Therefore, in the fourth test the pressure was increased. Microscopic evaluation of the product indicated the bulk of the product to be 3 to 5 microns.

Table 2-2. Jet-milled Resin 500 at Trost Company.*

Test No.	gm/h	Flow Rate SCFM	lb/in.^{2}/gage
1	160	18.4	100
2	100	18.4	100
3	150	90.6	80
4	300	50.1	275

Porosity measurements were performed on both compression-molded and isostatically molded billets from the jet-milled powder. Figure 2-3 shows the results from an uncured and cured compression-molded billet. Equivalent pore diameters in the uncured billet are significantly less than those observed in the cured billet. Results obtained from isostatically molded billets are shown in Figure 2-4. No significant reduction in pore diameter was noted.

An attempt was made to explore the effects of the contact angle (wetting angle) between mercury and compression-molded Resin 500. It was hypothesized that changes in the contact angle on curing could account for changes in the observed mean pore size after curing. If the wetting of the material by mercury increases (i.e., the contact angle decreases) without any change in the pore size distribution, then the mercury (in the porosimetry test) will penetrate the pores of the sample at a lower pressure; the pore size distribution will then appear to shift towards larger pore sizes.

The contact angle between a solid material and different liquids is a function of the surface tension of the liquid: as the surface tension of a liquid in contact with a solid surface is increased, its contact angle with the solid will increase and its wetting decreases.

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* Plastomen Products Division, Trost Mill Department; Garlock, Inc.; Friends Lane; Newtown, Pennsylvania 18940.

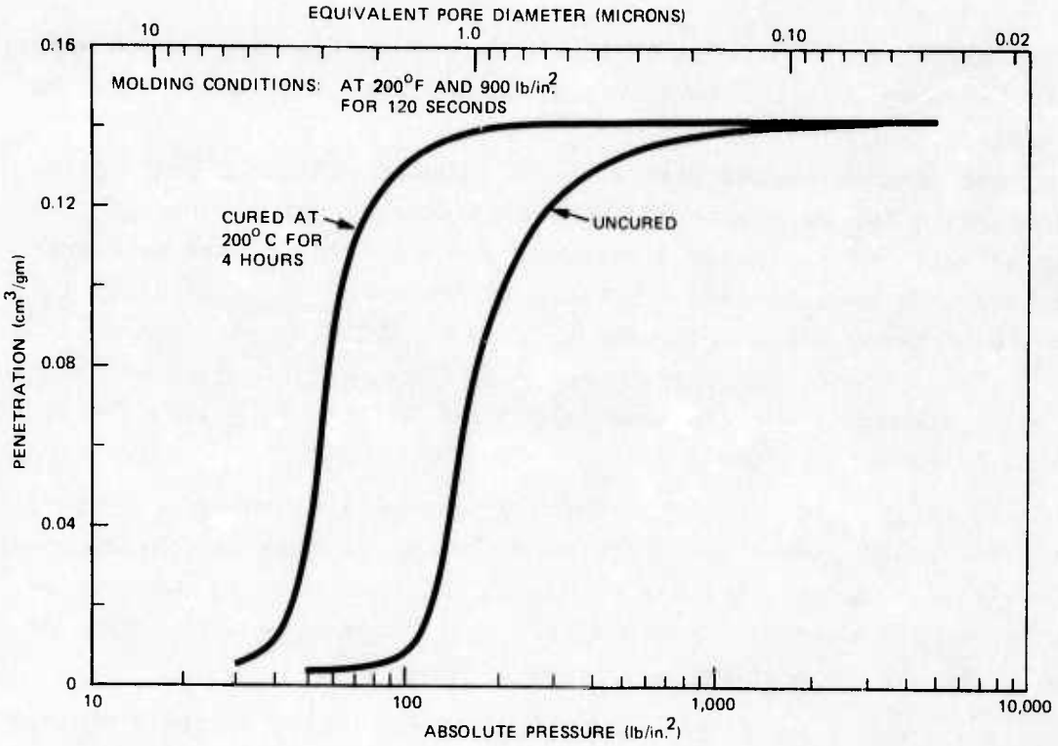

Figure 2-3. Pore-size distribution of compression-molded Trost ground Resin 500.

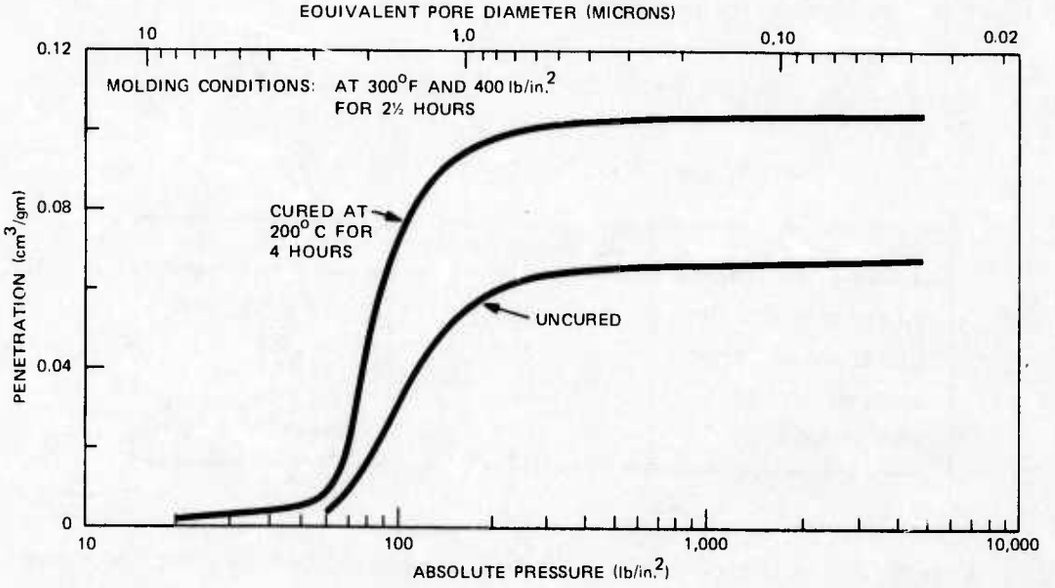

Figure 2-4. Pore-size distribution of isostatically molded Trost ground Resin 500.

By establishing the effects of curing on the contact angle with water, it is believed that the behavior of mercury with that surface may be deduced.

The contact angles with water of uncured and cured compression molded Resin 500 were measured photographically. After molding, the samples were not manipulated by hand but were handled with tweezers; otherwise, no special care was taken to avoid their contamination. The results of these tests indicated that no significant difference in wetting exists between the uncured material and material which had been cured in nitrogen, whereas materials cured in air or in vacuum were less wetted by water (see Table 2-3).

If these results can be directly extrapolated to wetting by mercury, one would expect the shift on curing to take place towards lower apparent pore sizes. This is in direct contradiction to observation. The hypothesis that the shift in pore size distribution on curing is due to changes in wetting is therefore incorrect.

Mixtures of Resin 500 powder and Skybond 701 or Kerimid binders were compression molded. These samples were prepared in an attempt to form the Monsanto polyamide-imide resins into porous structures having a mean pore size of about 1 micron. Irrespective of the ball-milling time (between 4 and 6 hours), porous structures with large pores were obtained, indicating that this material is difficult to grind and is similar to the Monsanto Resin 500 (see Figure 2-5).

Table 2-3. Order of wettability.

Contact angle of unbroken surface with water.

	Contact Angle	Wettability
nitrogen cured	65°	most wetted
uncured control	70°	↓
vacuum cured	102°	↓
air cured	110°	least wetted

A difference in pore-size distribution exists between compression-molded porous material and isostatically molded material (viz., Monsanto Polyamide-imide Resin 500). This difference is magnified on curing the

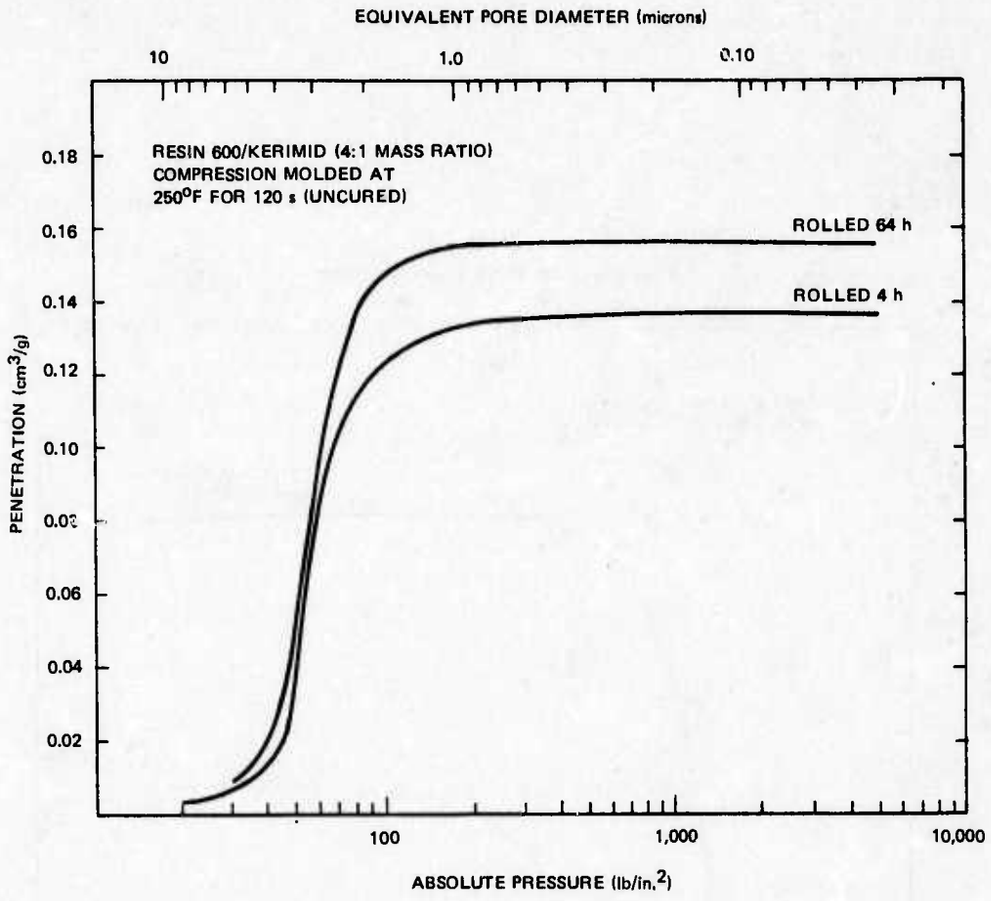

Figure 2-5. Pore-size distribution for various milling times.

porous material when the compression-molded material appears to increase significantly in pore size. An attempt was made to avoid this pore-size increase by compression molding the material for longer periods of time (1 and 2 hours) at the high pressure and temperature, instead of the standard 120-second period. This procedure did not reduce the differences between the final pore-size distributions (see Figures 2-6, 2-7, 2-8). It is felt that these differences are due to basic differences in the temperature/time history of the material during molding.

2.4 Incorporation of Solid Lubricants in the Retainer Material

The major task efforts during this reporting period were devoted to developing the broad-pore-peak material, compression molding and a single-component system. The bearing pair containing retainer impreg-

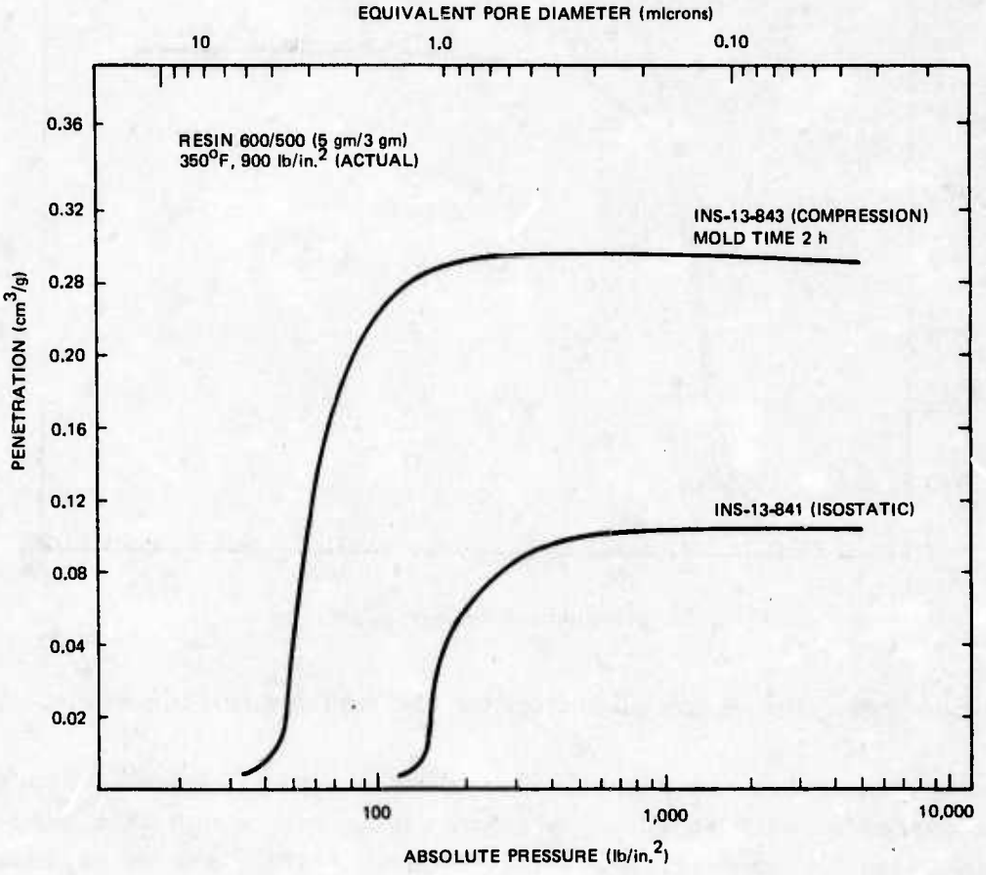

Figure 2-6. 600/500 mixtures pore-size distribution, 2-hour mold time.

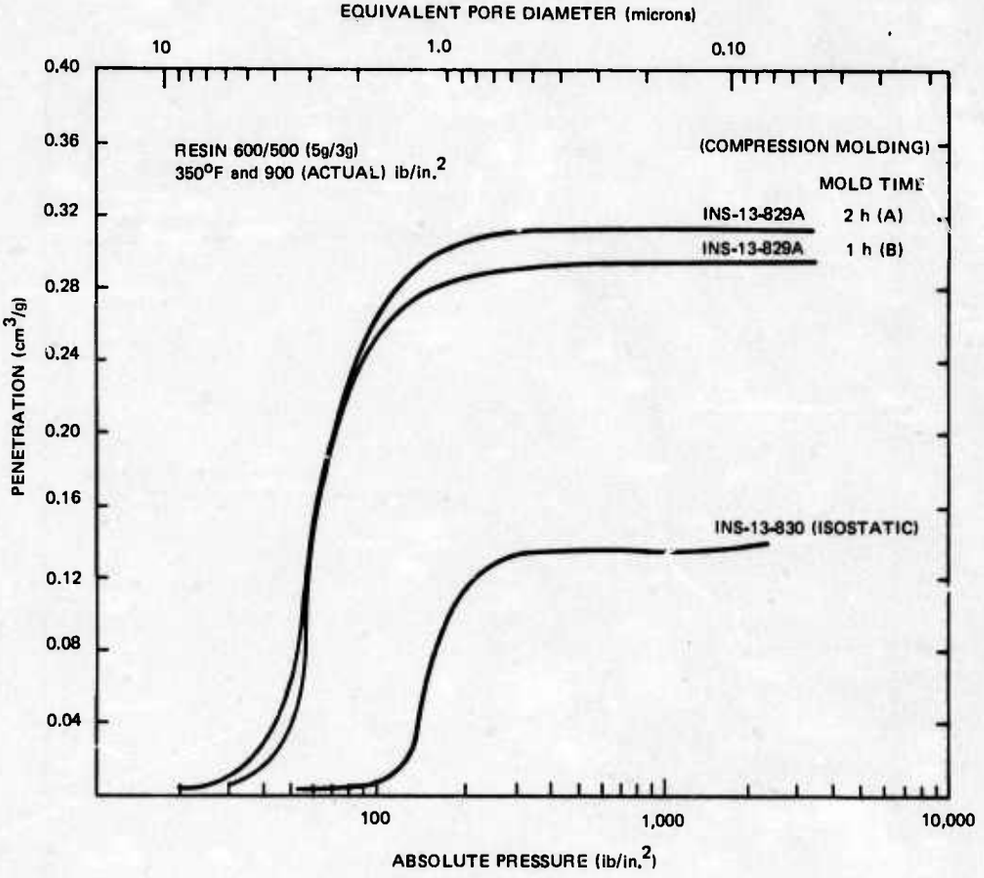

Figure 2-7. 600/500 mixtures pore-size distribution, 1- and 2-hour mold time.

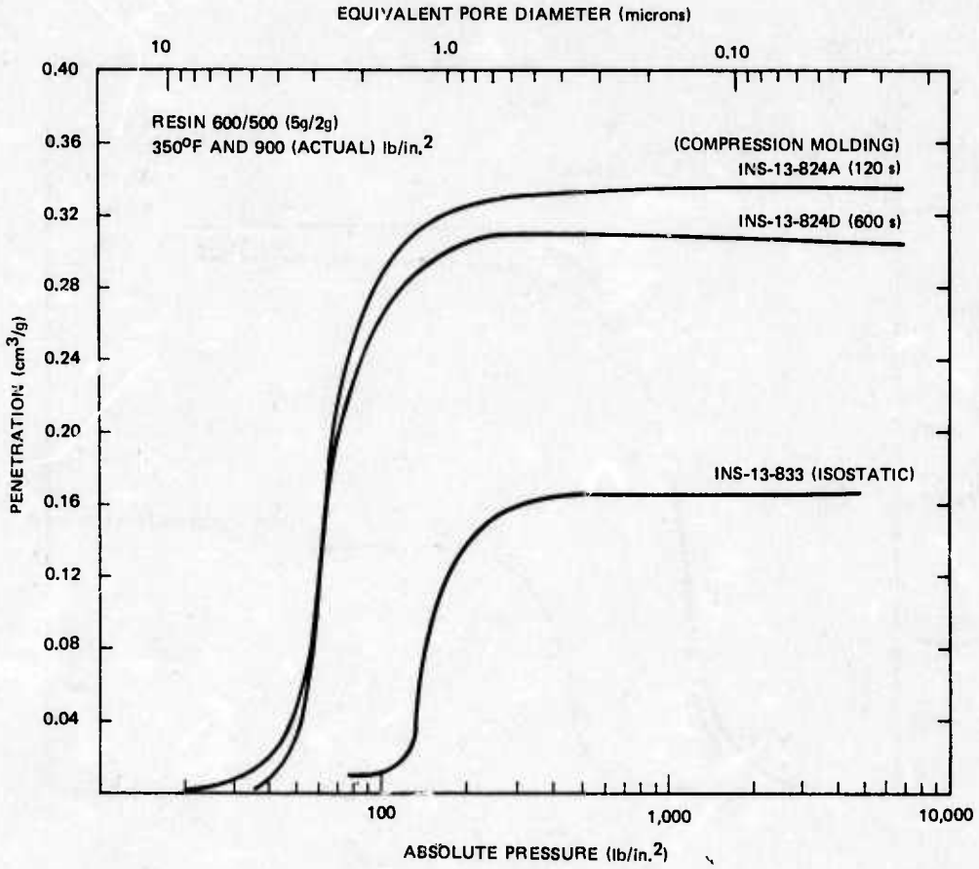

Figure 2-8. 600/500 mixtures pore-size distribution, 2- and 10-minute mold time.

nated with 1-percent molybdenum disulfide (MoS_2) continues to run, exhibiting satisfactory performance, and at the conclusion of this contract had accumulated 12183 hours.

An effort begun near the end of the contract and not completed was to determine if MoS_2-filled retainers exhibited greater strength when compression molded, contrasted with those which had been isostatically molded. Two samples were isostatically molded with 1-percent and 2-percent MoS_2. Three samples were compression molded with 1-percent, 2-percent, and 3-percent MoS_2. Porosimeter data are shown in Figures 2-9 and 2-10. It was planned to perform tensile tests on these samples, then to fabricate retainers, assemble them, and run bearings with them.

2.5 Summary

The goals established for this development task were not completely realized. There were, however, several significant accomplishments which strongly suggest the technical feasibility of the remaining goals.

The development of the polyimide material, currently being manufactured by Dixon Corporation as Meldin 9000, has had a positive impact on the G-200-gyro repair line at the Air Force AGMC where it has been incorporated. In addition, this material is being factored into the G-200 repair lines at the Naval Air Rework Facilities at North Island and Norfolk.

Work on the broad-pore-peak material has demonstrated feasibility of continuance of this task. Combinations of Torlon with various binders has produced material which shows promise of attaining the required pore volume, small slope to the porosity curves and range over the pore sizes, which is desirable.

Compression molding appears to be near completion. The parameters which determine the properties of the molded cured material are becoming better defined. It appears, at present, that a single component system may not be feasible, although more work should be done before a definitive statement is made.

Filling the material structure with a type of lubricant also shows promise. While the running of a single bearing pair for 12000-plus hours is not absolute proof, it does suggest that an effort of this sort may assist in providing the retainer stability required in a high-performance and/or high-reliability bearing. Parametric variation and more bearing running is necessary to determine the optimum configuration.

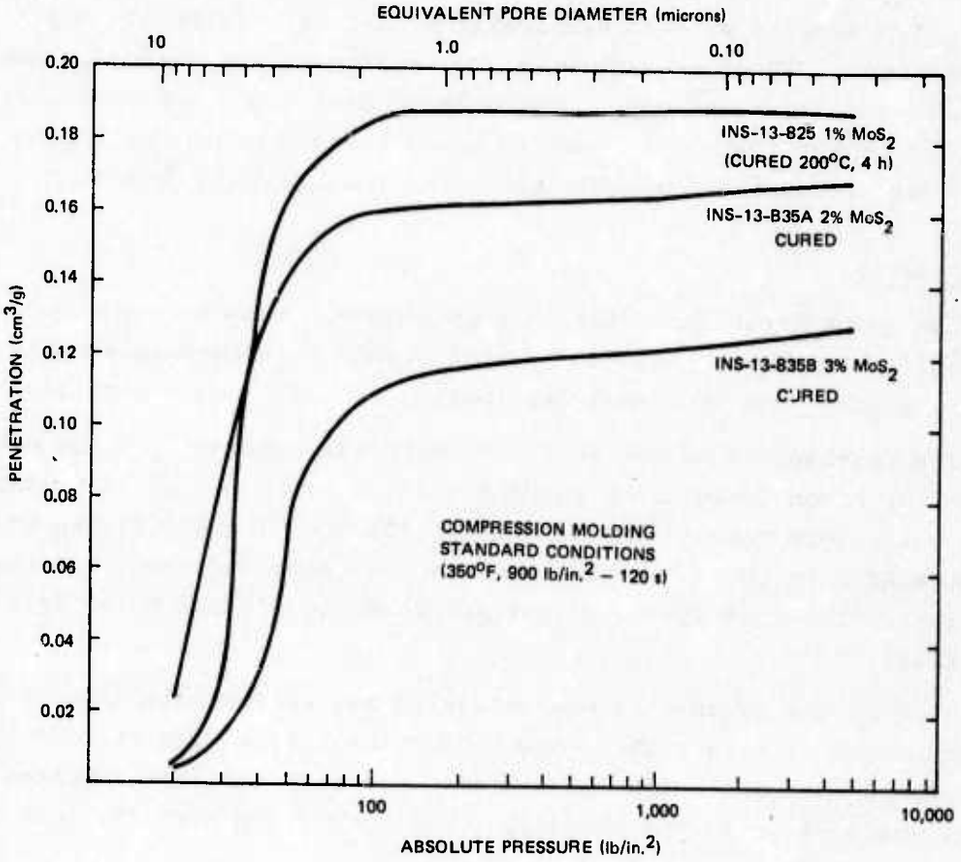

Figure 2-9. Pore-size distribution—
500 mixture, MoS_2-filled, compression molded.

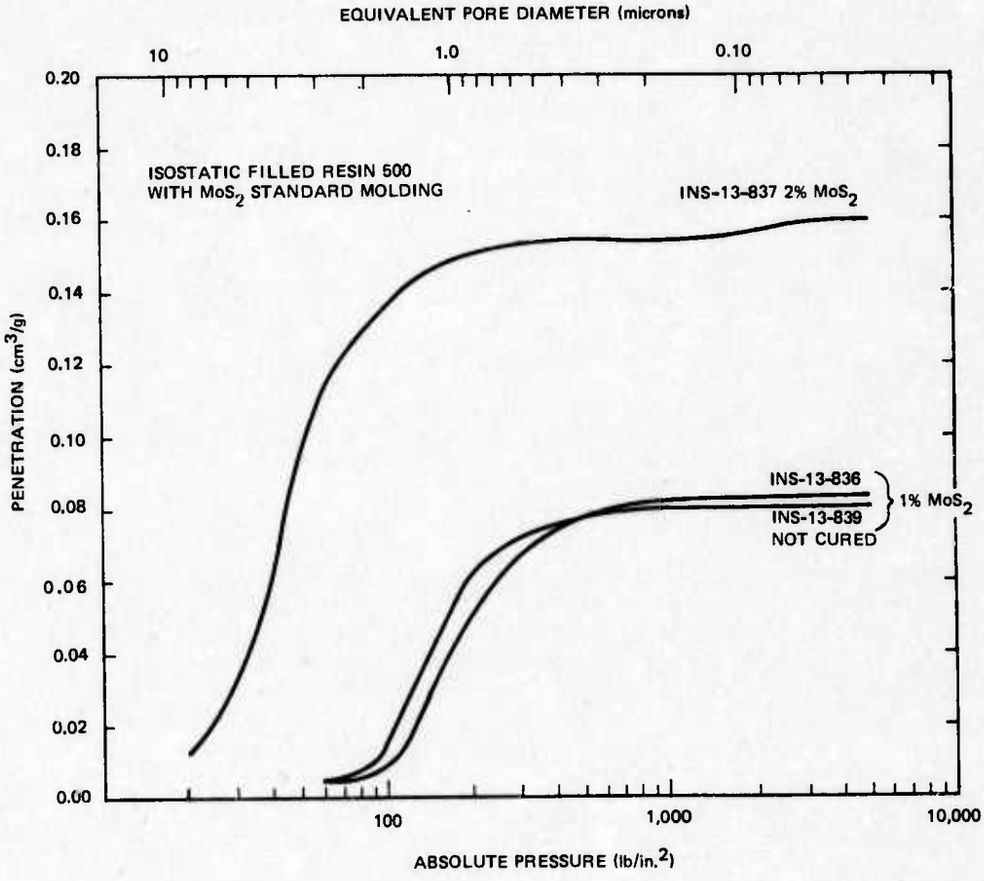

Figure 2-10. Pore-size distribution—
500 mixture, MoS_2-filled, isostatically molded.

PART B

ELECTRONIC-INSTRUMENT-SERVO-TECHNOLOGY INVESTIGATION

SECTION 1

INTRODUCTION

This is a 7-1/2-month report on the progress made under contract F33615-72-C-1335, Task 2.1, "Electronic-Instrument-Servo-Technology Investigation." In most cases, the studies that were conducted have been a continuing effort over the life of this contract. Therefore, for an in-depth discussion of the various topics presented, the references listed at the end of this section should be reviewed. The following is a brief introduction to the topics covered in this portion of the report.

Section 2 is a status report on the efforts being made to patent the Hypha Digital Phase-Locked Loop and to turn it into an integrated circuit.

Section 3 presents a discussion on the design of a Modified Hypha Dynamic Navstar Frequency Synthesizer. The beginning effort in this area was in the development of a Hypha Heterodyner. The dynamic Navstar frequency synthesizer is an extention of the Hypha heterodyner approach. It is anticipated that this design will provide a unique and low-cost implementation for producing the waveforms required for dynamic Navstar satellite simulation. A short discussion of the proposed Navstar system is presented as a means of defining the requirements for the synthesizer and as a means of justifying the modified Hypha approach. The circuit concepts in block diagram form are then described, followed by the present status of the task.

Section 4 presents an investigation of using Hypha technology in developing a Resolver-to-Digital (R/D) Converter. Linearity and accuracy data is provided with a description of many of the sources of error encountered. Also a brief write-up is given on the circuit design and its unique features.

Section 5 is a discussion of the Hypha Interpolator. This concept and circuit design provides a means of reducing the quantization error associated with pulse rebalance inertial instruments without degrading

other performance parameters. Contained in this section is actual data obtained from utilizing the interpolator circuitry, along with a power spectral density analysis of the results. This information shows that the concept does indeed perform to its expectations.

Section 6 presents the results from some experiments directed toward utilizing Hypha technology in the development of a Universal Servo Loop. This work is an offshoot of the Hypha interpolator task. Instead of having the Hypha circuitry working outside the control loop, it is now being placed within the servo system. Its flexibility and digital interface capability will, hopefully, provide an extremely useful building block for control systems.

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1. D. Cox, K, vanOpijnen, S. Rhodes, and L. Sutro, Hybrid Phase (Hypha) Processing and Data Conversion, Charles Stark Draper Laboratory Report E-2697, January 1973.

2. D. Cox, W. Daly, D. Gustafson, P. Hanks, W. Lee, K. vanOpijnen, W. Stonestreet, and L. Sutro, "New Techniques for Signal Processing and Conversion", Part B of Advanced Inertial Technologies, Technical Report AFAL-TR-73-124, Volume I, Air Force Avionics Laboratory, May 1973.

3. Duncan B. Cox, Jr., et al, Hypha Processing Technology Interim Report, Charles Stark Draper Laboratory Report R-796, March 1974.

4. Kenneth Bell, et al., "Electronic Instrument Servo Investigation", Part 1 of Advanced Inertial Technologies, Technical Report AFAL-TR-73-124, Volume II, Air Force Avionics Laboratory, November 1974.

SECTION 2

HYPHA DIGITAL PHASE-LOCKED LOOP

2.1 DPLL Patent Application

Two patent applications covering the Hypha digital phase-locked loop (DPLL) have been made by CSDL and are presently awaiting action by the U.S. Patent Office.

2.2 Integrated-Circuit DPLL

Putting the DPLL onto one integrated circuit (IC) would make the circuit much easier to use and would also result in performance advantages. A preliminary design for putting the DPLL onto one IC was described in AFAL-TR-73-124 Advanced Inertial Technology, Volume II. This work on the feasibility, desirability, and design of an IC DPLL has continued.

As a result of this work, it appears that CSDL, in conjunction with the RWN, AAI, and TEA groups at AFAL, will become involved in a program to put the DPLL onto a CMOS integrated circuit. The IC design will be done at CSDL and AFAL, and the actual fabrication will be done by RCA on a TCC-051, CMOS, 276-gate Universal Array. Figure 2-1 is a preliminary block diagram of the DPLL IC and Figure 2-2 is a preliminary logic diagram of the circuit to be integrated, as it would be on the chip.

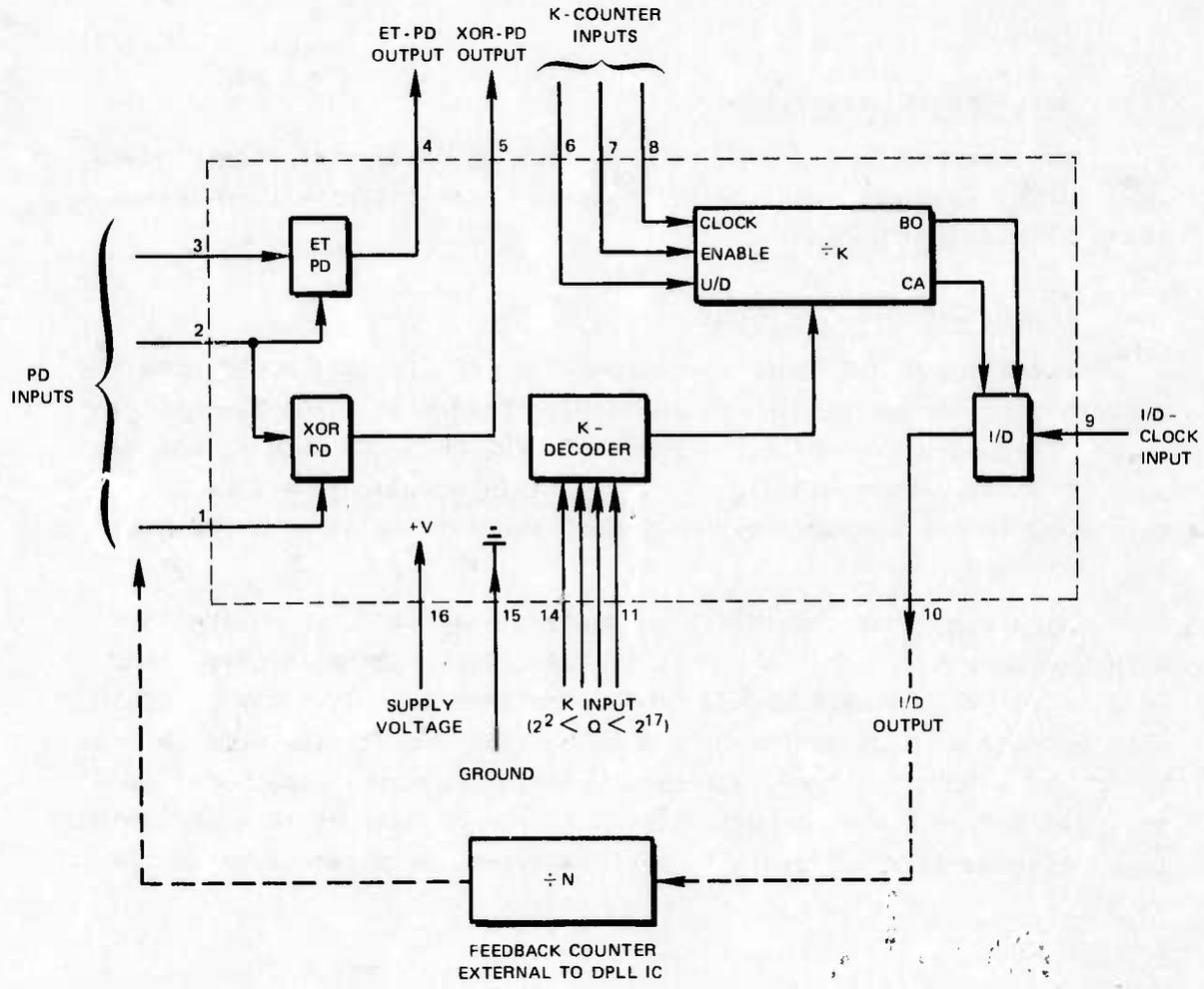


Figure 2-1. Partitioning for Hypha DPLL integration.

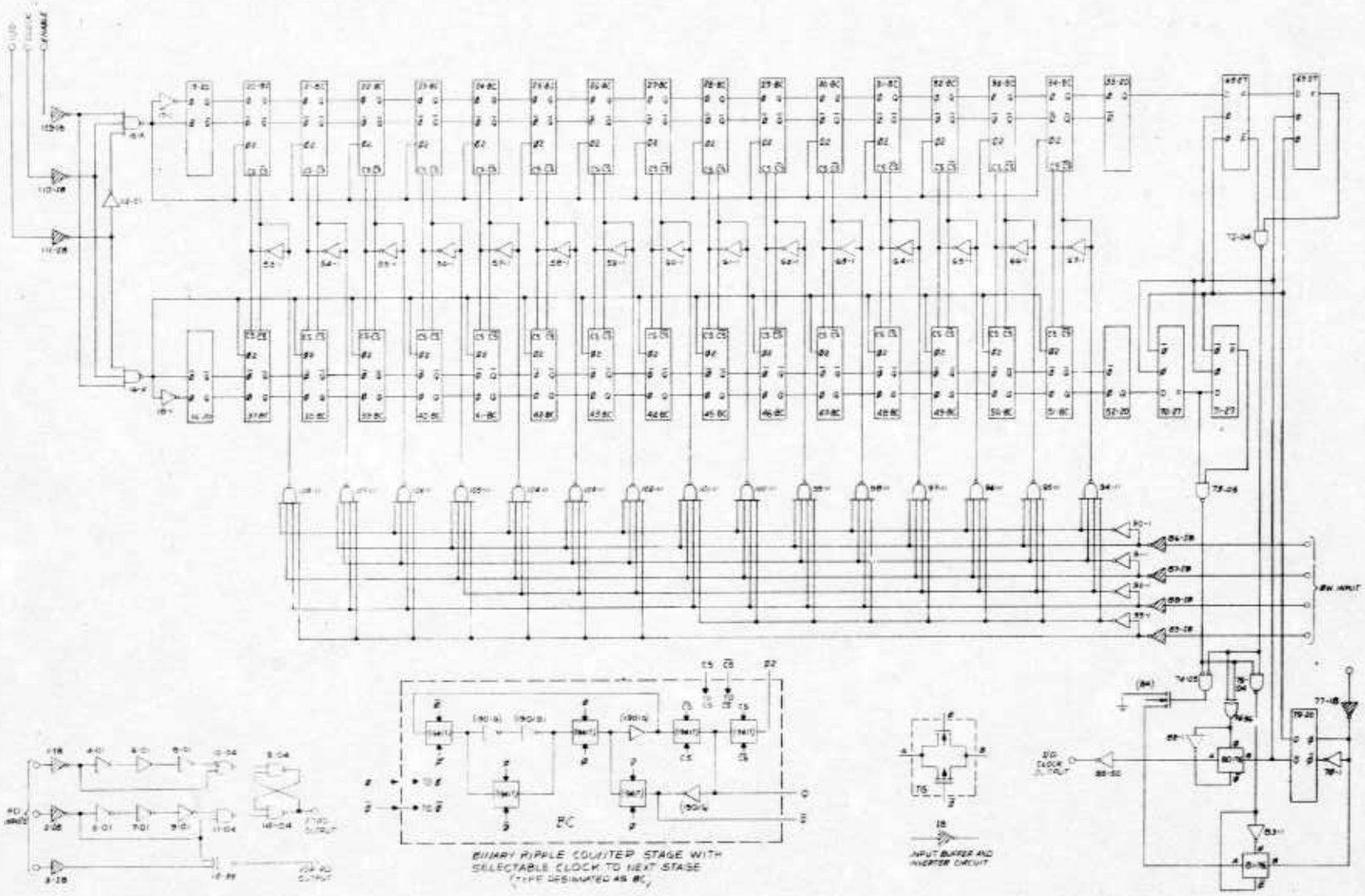


Figure 2-2. Preliminary logic diagram of DPLL integrated circuit.

SECTION 3

MODIFIED HYPHA DYNAMIC NAVSTAR FREQUENCY SYNTHESIZER

3.1 Introduction

The major emphasis since July 1974 in the area of frequency synthesis and heterodyning has been towards realization of hardware capable of being used in the test and evaluation of Navstar receivers. Certain new technology has been developed and an operational prototype of a Navstar frequency synthesizer is now under construction and evaluation.

Previous work on the subject of frequency synthesis has concentrated on the development of Hypha heterodyner technology. The synthesizer under development here is an extension of this approach.

The discussion of the current effort is best begun by looking at the relevant properties of the Navstar navigation system to which this synthesizer belongs.

3.2 Discussion

Each satellite in the Navstar system will generate a 10.23-MHz logic or code frequency and a higher 1575.42-MHz sinewave carrier frequency. The code frequency is used to drive an onboard code generator. The output of the code generator is used to bi-phase modulate the carrier prior to transmission and, thereby, spread the output frequency spectrum. A user must know this code in order to unscramble the carrier frequency. In normal operation of the system, both satellites and receivers will be moving, and this results in Doppler shifts in the carrier and code frequencies. Because the code frequency is contained as a modulation of the carrier frequency, the effective Doppler shifts of the carrier are 154 times higher than those of the code or, in other words, in the same ratio as the ratio of the two frequencies.

The task of the dynamic Navstar frequency synthesizer is to generate both the code and carrier frequencies and to simulate the frequency changes, i.e., Doppler shifts in both these waveforms. This

permits checkout of ground-based equipment without need for the satellites. One elementary approach to this problem is the phase-locked-loop system shown in Figure 3-1.

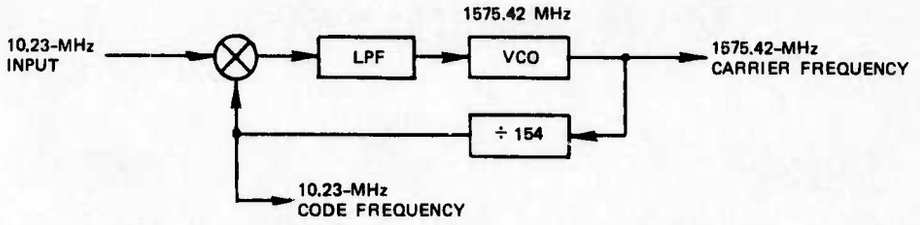


Figure 3-1. Elementary Navstar synthesizer.

Unfortunately, there are powerful reasons why this simple approach will not work. First, the Doppler or frequency shifts must be encoded directly on the 10.23-MHz input waveform and it is difficult to encode frequency shifts of the minimum magnitude required (10^{-4} Hz) directly on a 10-MHz waveform. It is advantageous to do this at a lower frequency and then heterodyne up to 10.23 MHz. Second, an IF frequency at 70 MHz is desired as the carrier frequency, later to be heterodyned to 1575.42 MHz. This means that the ratio of the two output frequencies will not be the same as the Doppler shifts encoded on them. The Doppler shifts must be in the ratio of 154 to 1, while the ratio of the two output frequencies will be 70 to 10.23. Hence, a simple divider chain will not suffice to generate one frequency from the other. Additionally, there are problems attaining VCO operation and counter-operation at 1575.42 MHz, and in attaining a high-resolution phase detector at 10.23 MHz. For these reasons, the approach discussed below is believed to be the simplest and most cost-effective method of accomplishing the task.

The major performance goals for the output waveforms are given in Table 3-1. This table shows that the dynamic frequency synthesizer will produce output waveforms of sufficient quality to enable a receiver to measure position to less than 1 foot and velocity to less than 0.01 foot per second. The unit will also be capable of simulating a 10-g acceleration and changing frequency 100 times a second. These figures for position and velocity are based on the conversion relationship of 0.63 foot per cycle at 1575.42 MHz. Frequency resolution is 1.2×10^{-4} Hz at 10.23 MHz and 154 times higher at 70 MHz, i.e., 1.9×10^{-2} Hz.

Table 3-1. Dynamic-Navstar-frequency-synthesizer output-waveform performance goals.

	10.23-MHz CODE SQUAREWAVE	70.0-MHz CARRIER SINEWAVE (TO BE HETERODYNED TO 1.57542 GHz)
AMPLITUDE	TTL squarewave	+7 dBm into 50Ω
DOPPLER SHIFT	0 ± 259.5 Hz in 2^{22} steps of 0.124 mHz	0 ± 39,961 Hz in 2^{22} steps of 19 mHz (corresponds to a minimum resolution of 0.011 ft/s at 1.57542 GHz).
PHASE RESOLUTION	One part in 308 of a full cycle (0.3 ns)	One part in 256 of a full cycle.
PHASE STABILITY	≤1-ns rms in a 100-Hz bandwidth over the simulation interval (≤1 ns corresponds to a position uncertainty of ≤1 ft)	One part in 64 rms when measured in a 1-Hz bandwidth over a measurement interval of 1 s (one part in 64 is equivalent to 0.01 ft at 1.57542 GHz. When measured over a 1-s interval, this permits resolution of 0.01 ft/s).
MAXIMUM FREQUENCY RATE (ACCELERATION)	3.25 Hz/s	500 Hz/s (this is approximately a 10-g acceleration).
MAXIMUM NUMBER OF CHANGES IN FREQUENCY IN 1 s	100	100

A block diagram of the entire synthesizer is shown in Figure 3-2. Each block in Figure 3-2 is described in detail beginning with the 5-MHz-to-40.92-MHz converter.

3.2.1 5-MHz-to-40.92-MHz Converter

Most high-quality high-stability frequency standards are located at even frequencies such as 5 MHz. The 10.23-MHz code frequency, however, is not directly related to a 5-MHz reference. So far as this

particular unit is concerned, it is desired that the synthesizer derive its frequency reference from a 5-MHz rubidium standard which the contractor already owns in the CSEL (Communication Systems Evaluation Laboratory) facility. In order to generate the code frequency, therefore, it is necessary to convert the 5-MHz CSEL reference to a 5.115-MHz Navstar reference. To do this, the approach illustrated in Figure 3-3 was developed. The standard technique for accomplishing the same task is shown in Figure 3-4.

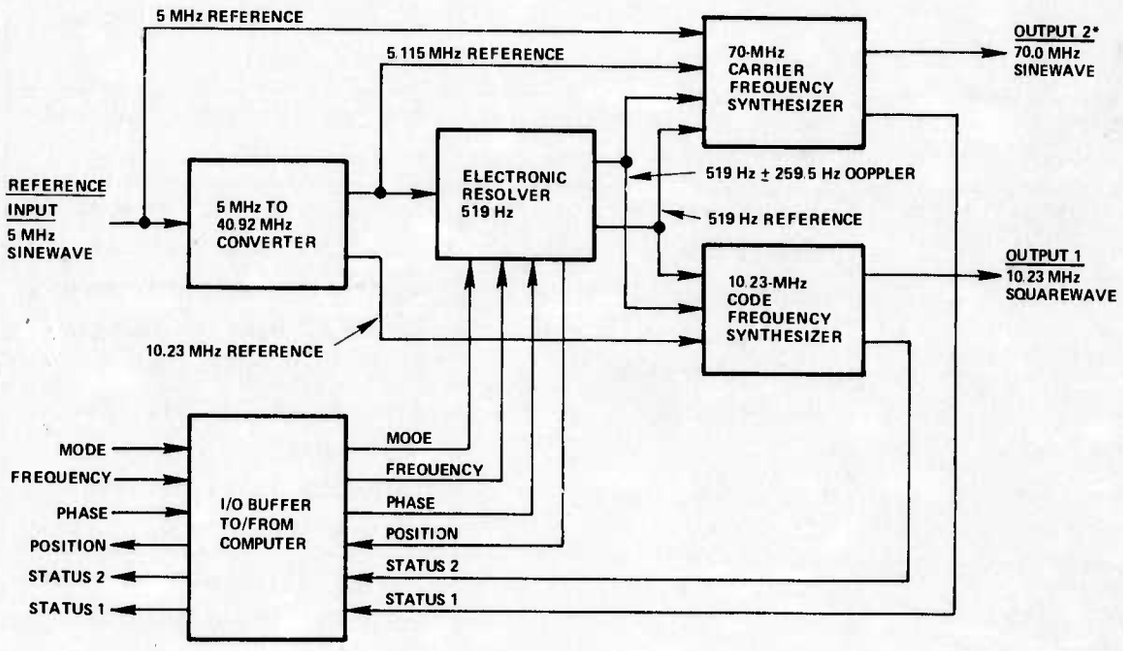


Figure 3-2. Dynamic Navstar frequency synthesizer.

The circuit of Figure 3-3 is a superior circuit and the concept underlying it is used throughout the synthesizer. The limitations of the circuit of Figure 3-4 lie in the limited dynamic range of the phase detector (PSD). Common gains for a phase detector are on the order of magnitude of 1 volt per radian. This means that even with a 60-decibel dynamic range, operation of the phase detector would remain linear and have resolution to about a milliradian. In this case, the 5.115-MHz

voltage-controlled crystal oscillator (VCXO) will have phase resolution no greater than $1.023(10^{-3})$ radian or about 1 radian. The circuit of Figure 3-3 heterodynes the 5.115-MHz VCXO down to lower frequencies rather than counts it down. This technique is conceptually superior, in this case, since a phase resolution of 1 milliradian in any of the mixers (the PSD of Figure 3-4 is also a mixer) in Figure 3-3 translates into the same resolution of 1 milliradian at the 5.115-MHz frequency; not more than a thousand times less, as in Figure 3-4. It can be said then, that the circuit of Figure 3-3 is more than a thousand times superior to the circuit of Figure 3-4 in terms of the phase integrity of the 5.115-MHz output frequency.

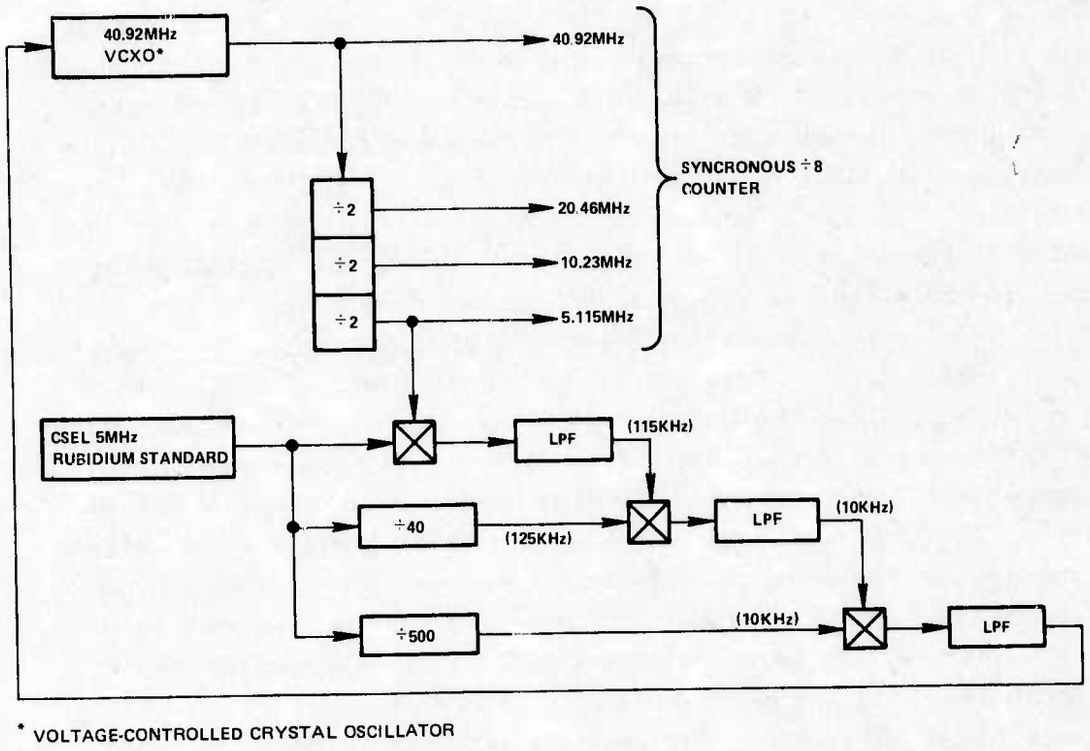


Figure 3-3. Conversion of CSEL 5-MHz rubidium standard to 5.115-MHz GPS frequency.

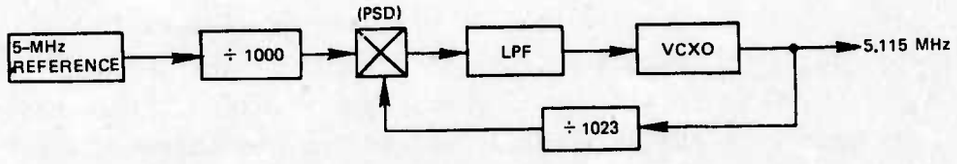


Figure 3-4. Standard 5-MHz-to-5.115-MHz converter.

3.2.2 Electronic Resolver

The electronic resolver is designed to digitally simulate the output waveforms of an analog resolver. In the case of the analog resolver, the resolver is excited with drive waveforms (usually from a few hundred to a few thousand Hertz). The resolver then provides a phase-modulating output signal at the drive frequency whose phase is proportional to the angular position of its rotating member relative to its stable member. A phase-locked loop is used to track this phase-modulating output and provide digital readout of the output resolver phase. When the resolver turns slowly, a constantly advancing phase appears at its output or, in other words, a small incremental frequency is added to the resolver output frequency. This in turn causes the VCO in the phase-locked loop to shift in frequency. This is the basic theory of operation of the dynamic Navstar frequency synthesizer with the exception that the analog resolver is simulated by an all-digital device called the electronic resolver. The output waveforms of the electronic resolver are logic squarewaves. A block diagram of the electronic resolver is shown in Figure 3-5. The adder and the 36-bit holding register generate the Doppler frequency of 0 ±259.5 Hz in 1.2×10^{-4}-Hz increments. The number at the output of the holding register is fed back to one of the two adder inputs where the selected number at the other adder input is added to it. This new number then appears at the output of the holding register immediately after the next clock edge, and the process repeats. In this way, it is possible to choose the correct increment and, hence, program the simulated angular speed of the resolver. The numbers at the output of the holding register correspond to the desired phase of the output resolver waveform. When a number appears at the frequency input in Figure 3-5, the output word from the holding register is an advancing phase with each number greater than the last by the chosen increment. The Sign input is used to convert the adder into a subtractor and produces a retarding phase, i.e., each output number is smaller than the last. Using the Mode input it is possible to bypass the adder and program the holding register directly with any absolute phase desired. This makes it possible to phase hop the output squarewave at any desired time to any desired phase. Even though the holding register is 36 bits long, only the 16 most significant bits are carried forward to represent the output phase. Moreover, only 39,424 out of a possible 65,536 (2^{16}) states are in use. The number 39,424 is a result of the desired phase resolution at 1575.42 MHz and is best illustrated using the circuit of Figure 3-1. A phase resolution of one part in 256 is desired at 70 MHz (representing

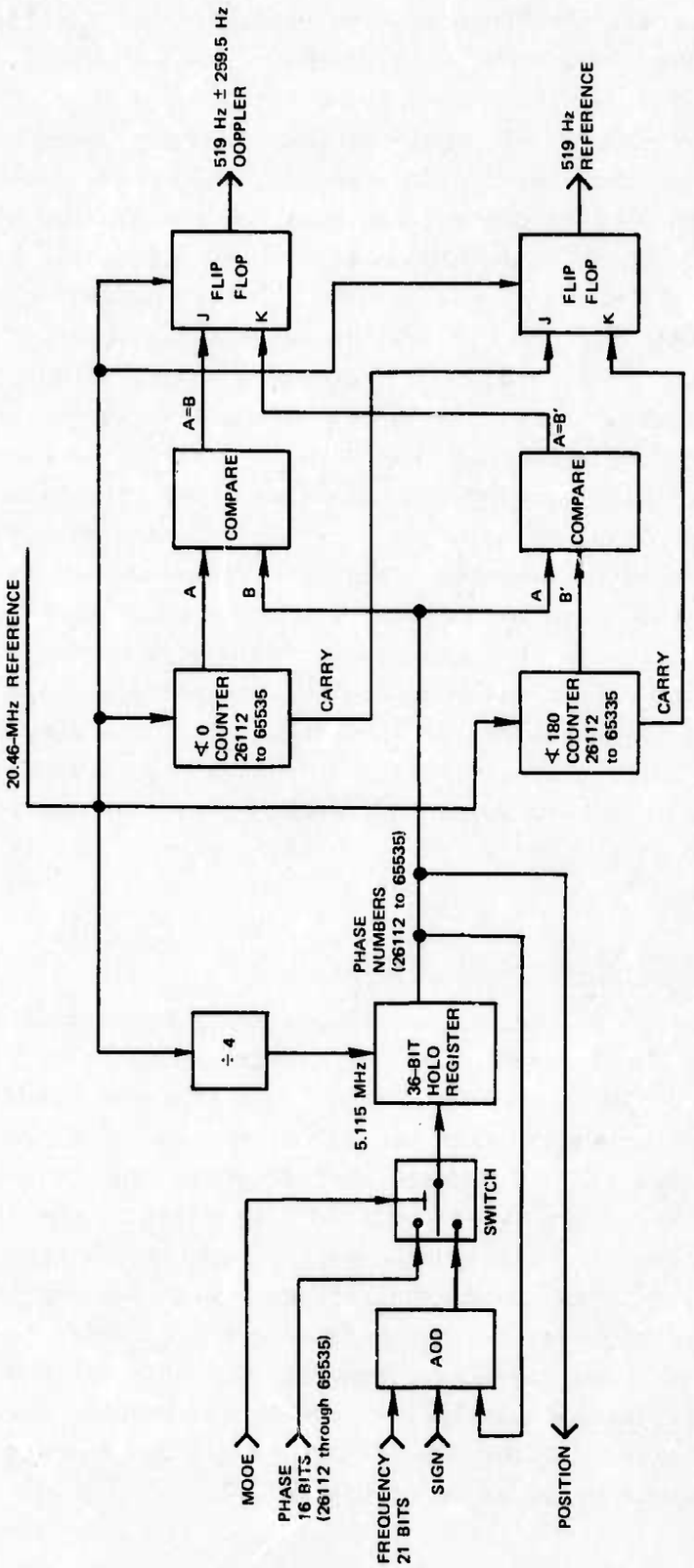


Figure 3-5. Electronic resolver.

1575.42 MHz). This translates into a phase resolution of 1/(256)(154) or 1/39424 at the lower frequency of 10.23 MHz. In other words, the electronic resolver divides its output phase into 39,424 equal quanta, and these are used to control the phase of the 10.23-MHz waveform. The holding-register phase does not control the 10.23-MHz phase directly, however. It is first used to control the phase of a 519-Hz waveform. This is accomplished, as shown in Figure 3-5, by comparing the holding-register phase with the phase of two forward counters operating at 519 Hz between the same maximum and minimum numbers as the holding register. When the phase of one of the forward counters passes through the holding-register phase (the holding-register phase rate is much slower) an edge of the 519-Hz output waveform is set via the output flipflop. The $\measuredangle 0$ and $\measuredangle 180$ forward counters cause both the rising and falling edges of the output waveform to be set consistent with the phase number in the holding register. When this phase number is slowly changing, it causes the edges in the 519-Hz Doppler waveform to change position with time; i.e., to phase modulate. This part of the electronic resolver can be thought of as a direct digital heterodyner where the advancing or retarding phase numbers at the output of the holding register (0 ± 259 Hz in 1.2×10^{-4}-Hz increments) are added to the 519-Hz offset frequency. The reason for providing this offset frequency and for providing the unmodulating 519-Hz reference will become clear in the remaining discussion.

3.2.3 10.23-MHz Code-Frequency Synthesizer

The function of this circuitry is to add the Doppler shifts contained in the 519-Hz Doppler output of the electronic resolver to the 10.23-MHz reference while, at the same time, rejecting the 519-Hz offset frequency. The block diagram of the circuitry used to accomplish this is shown in Figure 3-6. A two-step procedure is used to achieve the final result. First, the 519-Hz reference is added to the 10.23-MHz reference, and then the 519 ± 259.5-Hz Doppler is subtracted from the first sum. The result is the 10.23-MHz reference with the Doppler frequencies superimposed upon it. Two oscillators are needed to accomplish this task. The first oscillator runs at 10.230519 MHz and is used to heterodyne the second oscillator down to the Doppler frequency output of the electronic resolver. An alternate way to generate the the 10.230519-MHz frequency is shown in Figure 3-7.

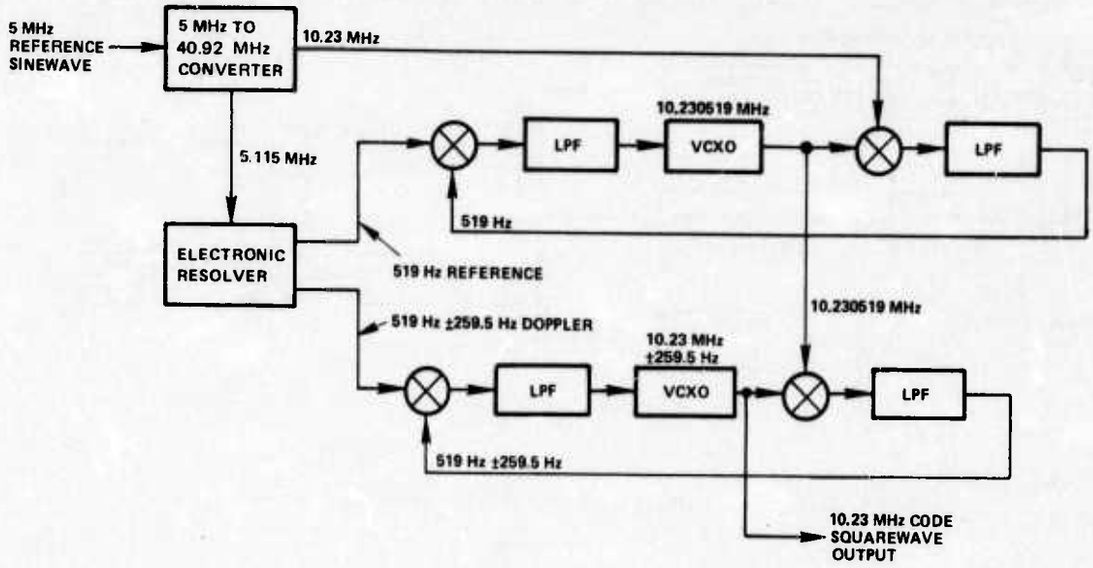


Figure 3-6. 10.23-MHz code-frequency synthesizer.

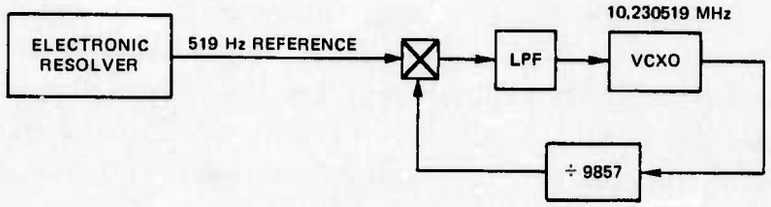


Figure 3-7. Standard 10.230519-MHz synthesizer.

The circuit of Figure 3-7 has all of the shortcomings of the circuit of Figure 3-4 as discussed in Subsection 3.2.1. The circuit of Figure 3-6 avoids these pitfalls and can be viewed as a balanced heterodyne approach, as illustrated by Figure 3-8.

Considering only the solid lines, Figure 3-8 shows a 10.230519-MHz oscillator mixing with both the 10.23-MHz reference and the 10.23-MHz VCXO. This yields two low-frequency 519-Hz waveforms. Moreover, if these two 519-Hz waveforms are phase-locked together (through the action of the feedback loop around the 10.23-MHz VCXO), the VCXO will be locked to the 10.23-MHz reference. Hence, it is possible to maintain two

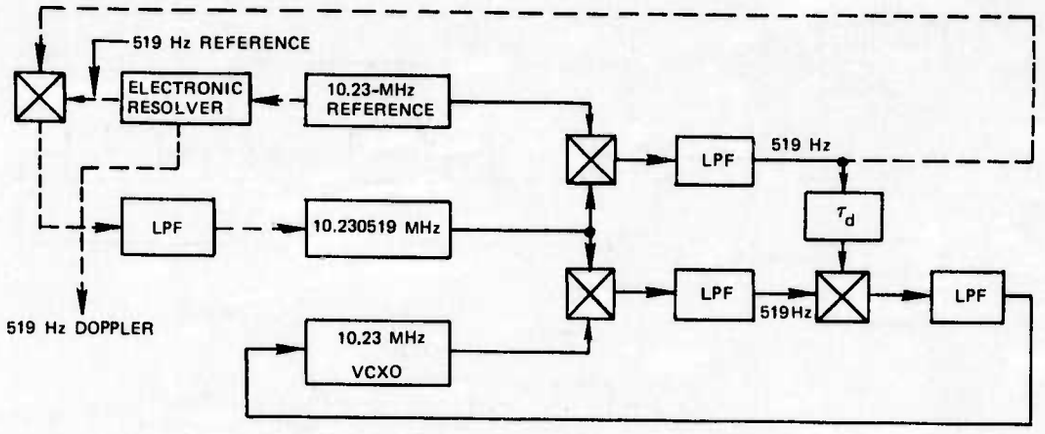


Figure 3-8. Balanced heterodyne synthesizer.

high-frequency 10.23-MHz oscillators in phase lock by going through a two-step process. Rather than beat these two waveforms against each other as in a conventional phase detector, a third oscillator can be used to recover an intermediate frequency between dc and 10.23 MHz (in this case 519 Hz). The system is immune to small frequency shifts in the 10.230519-MHz oscillator since it affects both 519-Hz waveforms equally. Moreover, any compensating nonideal properties, such as temperature drift, in the mixers will cancel. The advantage of this approach is that insertion of a delay (τ_d) into the circuit at the 519-Hz frequency will maintain the two 519-Hz waveforms and, hence, the two 10.23-MHz waveforms at some relative phase difference. If the value of this delay changes with time, there will be a frequency difference between the two 10.23-MHz oscillators (with the 10.23-MHz VCXO being the one that has changed).

In order to insert this time delay, it is convenient to have the 10.230519-MHz and 519-Hz frequencies phase-locked to the system frequency standard. To accomplish this the circuitry shown by dotted lines in Figure 3-8 is added.

Essentially, the 10.230519-MHz oscillator is replaced by a narrow-deviation VCXO centered about 10.230519 MHz. The 519-Hz beat note from mixing the 10.230519-MHz VCXO with the 10.23-MHz reference is phase detected against the 519-Hz electronic-resolver reference output and the error signal fed back to the 10.230519-MHz VCXO. The time delay, τ_d, is introduced by having the 10.23-MHz VCXO (after heterodyning to 519 Hz) track the 519-Hz Doppler output of the electronic resolver (not shown in

Figure 3-8). This results in the setup of Figure 3-6. Using this circuit, the full amount of the Doppler shifts in the 519-Hz waveforms are passed along to the 10.23-MHz waveforms. Hence, the phase and frequency of a high-frequency (10.23 MHz) waveform is controlled by the phase and frequency of a low-frequency waveform (519 Hz).

The 519-Hz offset frequency introduced by the electronic resolver permits loop bandwidths to be kept high, e.g., 100 Hz. Without this offset frequency, the bandwidths would be related to the minimum Doppler shifts of 10^{-4} Hz and the system would be incredibly slow. The performance goals for this portion of the circuitry are given in Table 3-1.

3.2.4 70-MHz Carrier-Frequency Synthesizer

The function of this circuit is to generate the 70-MHz carrier frequency which will ultimately be heterodyned to 1575.42 MHz. One major difference in this circuitry compared to that of Subsection 3.2.3, is that the Doppler shifts in the 519-Hz electronic-resolver output must be multiplied by 154 before being added to the 70-MHz carrier. At the present time, there are two variations of this circuit under evaluation. They are shown as Figures 3-9 and 3-10.

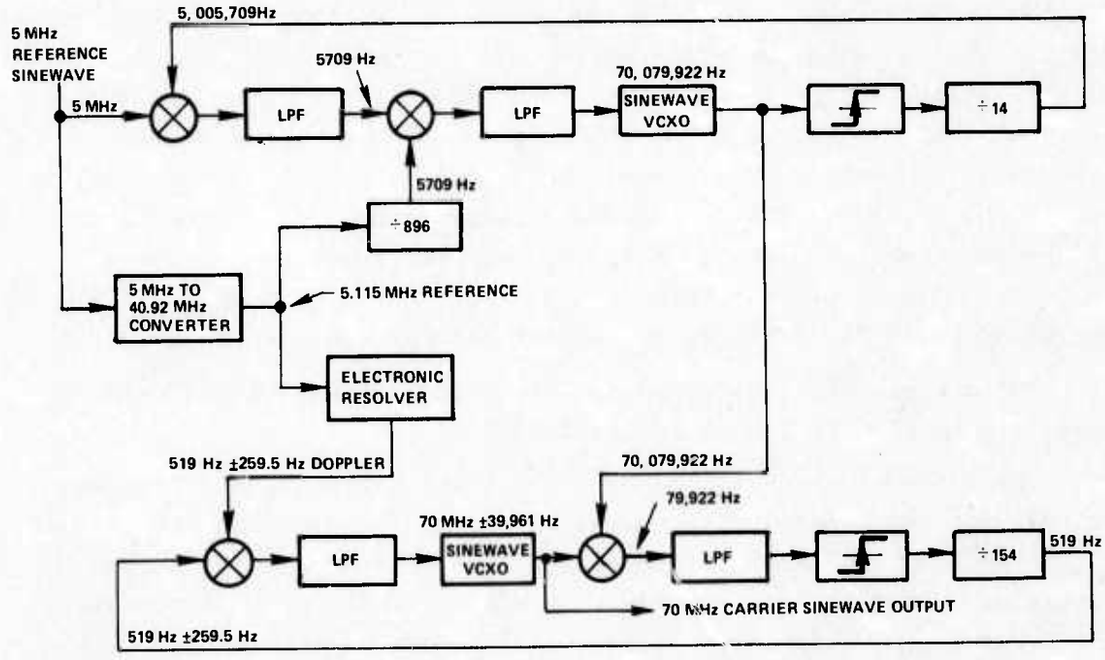


Figure 3-9. 70-MHz carrier frequency synthesizer, Alternative 1.

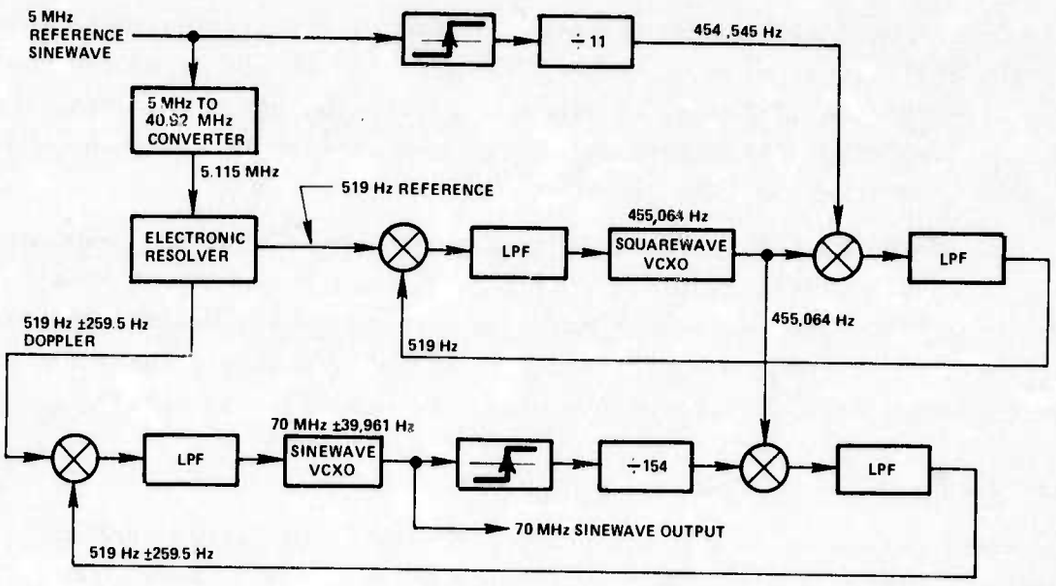


Figure 3-10. 70-MHz carrier frequency synthesizer, Alternative 2.

Figure 3-10 bears the most resemblance to the 10.23-MHz synthesizer of Figure 3-6. The major difference lies in the presence of the ÷154 following the 70-MHz VCXO and the ÷11 following the 5-MHz input reference. The ÷154 is necessary to produce the multiplication by 154 of the Doppler shifts. This in turn necessitates the ÷11 following the 5-MHz input in order to synthesize a reference frequency identical to the center frequency of the 70-MHz VCXO after division by 154. In other words, 5 MHz/11 = 70 MHz/154. The operation of this loop is then identical to that of the 10.23-MHz loop described in Subsection 3.2.3. The only difference is the change from the 10.23-MHz reference to a 5 MHz/11 reference. The heterodyne VCXO in this loop runs at 5 MHz/11 + 519 Hz instead of 10.23 MHz + 519 Hz as was the case in Subsection 3.2.3.

The difference between the implementation of Figure 3-10 and Figure 3-9 is illustrated in Figure 3-11.

The difference between Alternative 1 and Alternative 2 lies in the order of the heterodyning operation versus the division operation. The 70-MHz frequency must be reduced to the 519-Hz frequency through a division by 154 and heterodyning. However, either operation could come first as shown in Figure 3-11. In the case of Alternative 1, the the synthesis of the frequency necessary to heterodyne the 70 MHz

to 79,922 Hz is more complicated than synthesis of the 455,064-Hz frequency necessary for the same purpose in Alternative 2. However, the low-frequency result (519 Hz) is a squarewave in Alternative 1 and a triangle wave in Alternative 2, and the squarewave is preferred since it makes the final phase detection much easier.

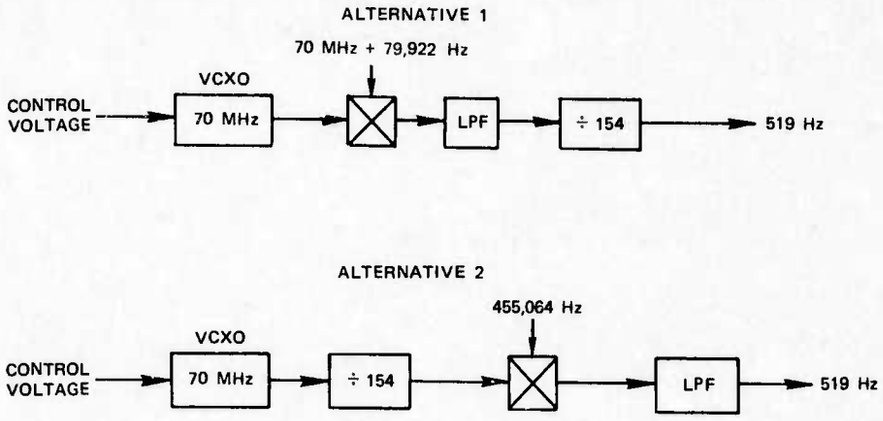


Figure 3-11. Reduction of 70 MHz to 519 Hz for Alternatives 1 and 2.

The final approach selected will be the one which best meets the performance goals set forth in Table 3-1.

3.2.5 Computer Interface I/O

At present, very little has been done here, and system specifications must be firmed up prior to defining this area. The I/O will provide the usual services of noise immunity, buffering of data, and ensuring compatibility of data formats. A key question still unanswered pertains to how "smart" the I/O should be. Depending on how much direct control the computer can exercise, it will be necessary to provide either greater or lesser capability in the I/O. At one extreme, the I/O could have stored subroutines permitting a navigation simulation (essentially a preprogrammed set of Doppler frequencies) to be selected with only a few instructions from the computer. At the other extreme, the computer would have to command each and every change in the Doppler frequencies. This question should move toward resolution in the next few months.

3.3 Current Hardware Status

At present, the electronic resolver has been fabricated, tested, and meets all performance goals. The 10.23-MHz code-frequency synthesizer has been fabricated and is in the evaluation process. The 70-MHz portion is being designed, as is the 5-MHz-to-40.92-MHz converter. It is expected that an operational prototype should be complete by early June.

SECTION 4

HYPHA RESOLVER-TO-DIGITAL CONVERTER

4.1 Introduction

In many computer-controlled processes or vehicle systems there is an input/output processor to encode, sequence, and process the data. These converters are completely digital; hence, conversion of resolver information to digital words must be made before the I/O processor may be remotely controlled. The Hypha resolver-to-digital (R/D) converter being simple, small, and inexpensive, therefore, becomes an attractive alternative to existing technologies. Its flexibility and digital interface capability provides a means of preprocessing and filtering the input analog information.

The principal objective of this investigation was to try out ideas that may lead to extended resolution and improved accuracy in Hypha processing systems, without additional circuitry. Careful attention was paid to minimize external influences that introduce errors in the phase-locked loop. Hence, remaining errors and noise sources are expected to be located within the loop.

4.2 Design of a Demonstration PLL R/D Converter

The demonstration PLL R/D converter (see Figure 4-1) uses a 32-step pedestal-weighted FET phase-to-analog voltage converter which is the phase-sensitive dectector (PSD) in the system. The output signal is summed into the input of an active low-pass filter. This stage amplifies and filters the error signal, which feeds it to a 74S124 Schottky voltage-controlled oscillator (VCO) clocking a 17-bit binary synchronous counter. The countdown contains phase information when strobed out, and also sets the timing for the phase detector. A master clock oscillator is used to derive the system frequencies. The 400-Hz sinusoidal- and cosinusoidal-resolver drive signals are generated from this master clock as well as the synchronous low-frequency strobe to latch the phase data.

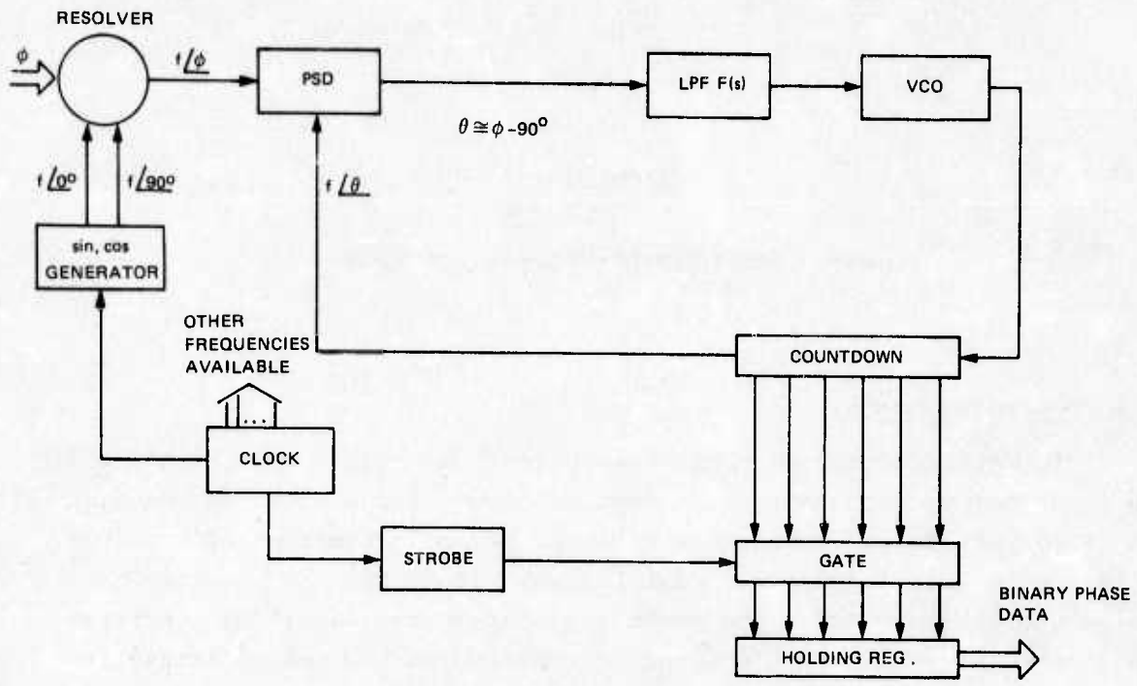


Figure 4-1. Resolver-to-digital converter.

The standard resolver is driven using sine and cosine 400-Hz waveforms. The resolver output is a phase-modulating sine and cosine waveform which is fed directly to the 32-step pedestal phase detector. The analog output of this circuit is directly proportional to phase difference between the analog resolver output waveforms and the phase-locked-loop-feedback waveforms.

4.3 Investigation Results

4.3.1 Errors and Their Sources

To date, jitter in the 14th bit limits the resolution of the R/D converter. A number of spectrum plots and tests were made to locate the source of the jitter. This noise appears in the low-pass-filter (LPF) and VCO outputs, and is also visible as jitter in the 14th bit of the binary output information. Spectrum plots demonstrated that the frequency content of all three of these waveforms is essentially the same. There is a sizable frequency component at 100 Hz, which is due to the strobe. Hence, the strobe frequency must be moved down to one tenth of the loop bandwidth—approximately 10 Hz or less. This allows adequate settling time between data points, as it takes seven to ten time constants for a servo loop to settle within 1 LSB. The

major higher-order harmonics of the LPF output are located at f_0, $2f_0$, $4f_0$, and $8f_0$ with a minor peak at $3f_0$. Some of these even harmonics are a direct result of the PSD output, which is imperfect and contains even harmonics. Improving this PSD would involve ordering custom resistors and matched FET switches, to eliminate the present tolerance problems.

A simplified 32-step pedestal multiplication is used in the PSD. This circuitry has been shown to function well and contains a minimal amount of parts.

The top waveform shown in Figure 4-2 is the jitter in the LPF output, which shows up as ripple in the 14th bit. The bottom waveform is the +5-Vdc VCO-power-line spectrum. There is a major 60-Hz component in the +5-Vdc spectrum plot, but none in the LPF plot. Hence, it can be said that this is not a source of phase error in the PLL.

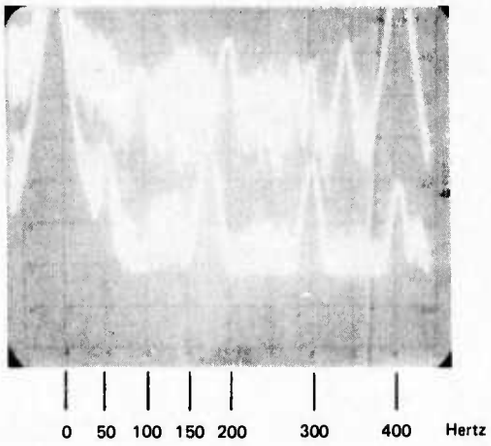


Figure 4-2. Noise/jitter spectrum plot.

4.3.2 Resolver Testing

Linearity testing of the R/D converter was accomplished with the aid of a resolver bridge which served as the reference standard for precisely setting the output of a resolver to specific electrical angular settings. The resolver outputs, K sin θ and K cos θ, were connected into the bridge with a preset angle of ϕ. The angular position of the resolver's rotor, θ, was varied until the bridge null output was minimized, indicating that $\theta = \phi \pm 0.1$ arcsecond. ϕ was varied over the

range of 0 to 360 degrees in 10-degree increments as the resolver angle θ was read by the R/D converter. This procedure provides a means of accurately testing the R/D circuitry and eliminates the problem of errors within the resolver itself.

4.3.3 Resolver Excitation

For purposes of testing and providing excitation for resolvers, a digitally driven sine and cosine generator was constructed and the purity of the resultant waveform was measured. Relative to the fundamental component, the second harmonic was attenuated 30 decibels, the third harmonic was attenuated 12 decibels, and the fifth harmonic was attenuated 35 decibels.

There are two contributing sources of error[1]* in an R/D converter which have been eliminated, as much as possible, in the initial set-up of the resolver-drive waveforms:

(1) Amplitude mismatches.

(2) Phase-shift problems.

If the excitations to the resolver and the gains of the PSDs are mismatched by ε_1 and ε_2, respectively (see Figure 4-3), then the conversion error is

$$\theta_e = \frac{\varepsilon_1}{2} \cdot \frac{\varepsilon_2}{2} \sin 2\phi \text{ radians}$$

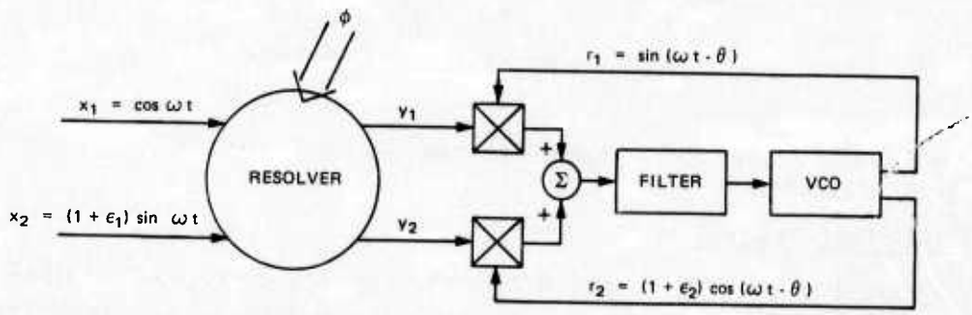


Figure 4-3. The relative immunity to mismatches in excitation amplitudes and detector gains.

* Superscript numerals refer to similarly numbered references in the List of References.

If resolver excitations are out of quadrature by $\delta_1/2$, the conversion error is dependent on $\delta_1/2$, as represented by the expression

$$\theta_e = \text{conversion} = \frac{\varepsilon_2}{2} \times \frac{\delta_1}{2} \cos 2\phi \text{ radians}$$

4.3.4 Phase Noise and Linearity

Figures 4-4 and 4-5 are error plots showing the difference between the electrical resolver angle, as determined by the resolver bridge, and the strobed-out PLL angular measurement, i.e.

$$\varepsilon = \phi_R - \theta_e$$

where

ϕ_R = electrical angle set in resolver via resolver bridge

θ_e = electrical angle read on PLL output

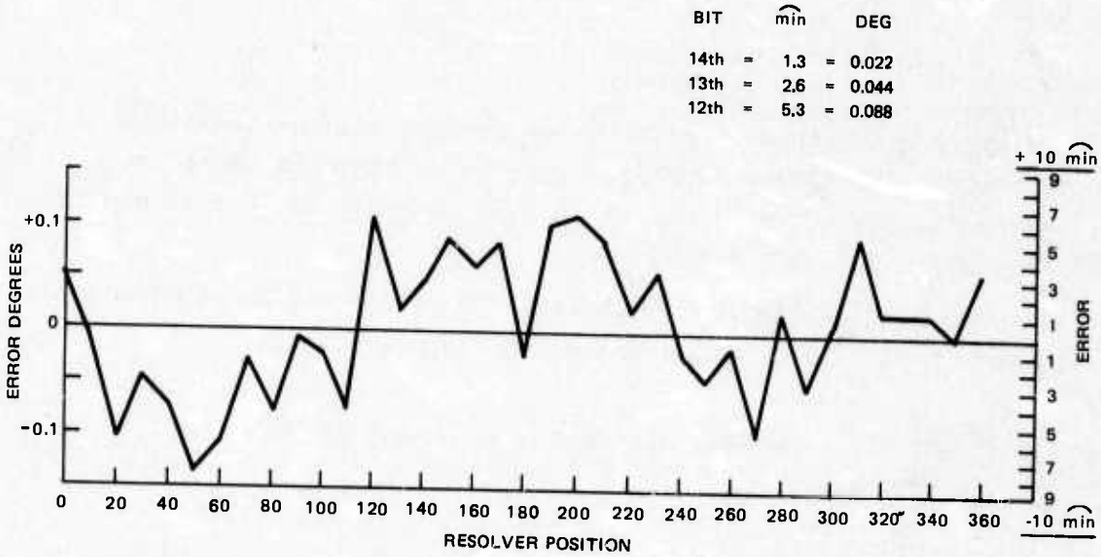
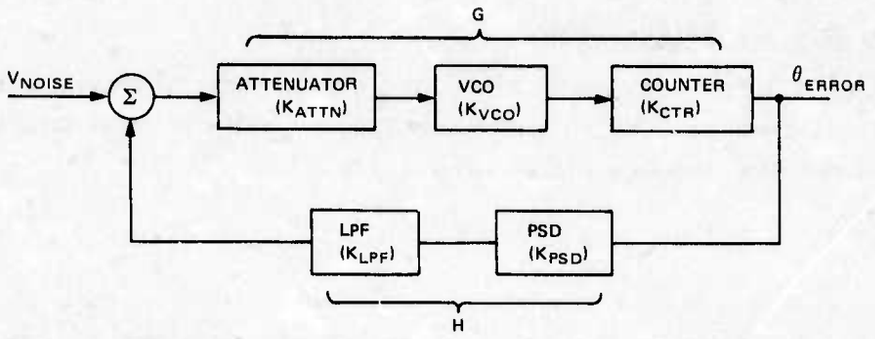


Figure 4-4. R/D converter error plot for Clifton resolver (32-step pedestal; Schottky VCO).

Figure 4-4 shows that a ±0.1-degree peak-to-peak error exists in the R/D converter, which translates to 12 bits of good linearity. The error plot also has embedded in it a 1-ϕ error (one cycle error in

a total of 360 degrees) due, at least in part, to a 400-Hz ripple in the LPF output. This 1-ϕ error can be predicted, and the solution is to move the Bode plot cross-over point back, to allow the PLL to attenuate 400 Hz more effectively.



$$\frac{\theta_{ERROR}}{V_{NOISE}} = \frac{G}{1 + GH} = \frac{K_{ATTN} \cdot K_{VCO} \cdot K_{CTR}}{1 + K_{LPF} \cdot K_{PSD} \cdot K_{ATTN} K_{VCO} \cdot K_{CTR}}$$

Figure 4-5. Phase-locked loop with noise input.

If the R/D converter has noise- or error-producing harmonics at the LPF output, the amount of ripple that is produced in the output data can be calculated using the block diagram and Bode plot shown for a 400-Hz ripple in Figure 4-5.

The fundamental ripple contribution is calculated by picking gains off the Bode plot at 400 Hz for these functional blocks.

$$\left.\frac{\theta_e}{V_N}\right|_{f_0=400} = \frac{\frac{1}{2} \times \frac{1}{40}}{1 + \frac{1}{200} \times 1 \times 10} \approx 0.0125 \text{ rad/V}$$

$$= 0.72^{\circ}/\text{V}$$

$$= 43 \widehat{\text{min}}/\text{V}$$

The ripple content of the LPF output was measured to be 40 millivolts peak to peak with its primary component at 400 Hz, which would yield a peak-to-peak error contribution of 1.72 arcminutes. However, it can be seen from the error curve shown in Figure 4-4 that the 1-ϕ error is at least nine times the error caused by the ripple at the LPF

output. This indicated that this error source is no longer the major contributor of angular error in this circuit. It is suspected that the major source of error is now a 400-Hz pick-up on the inputs to the R/D converter.

4.3.5 Temperature Performance

The PLL was put into an oven and raised from a room temperature of 30°C to 90°C. The resultant error plots shown in Figures 4-6 and 4-7 contain excursions of ±0.15 degrees for 11 bits of accuracy; the components used were not selected for properties that would minimize thermal effects. The results indicate that this phase-locked-loop circuit could be redesigned using military-specification parts and temperature range without major difficulties.

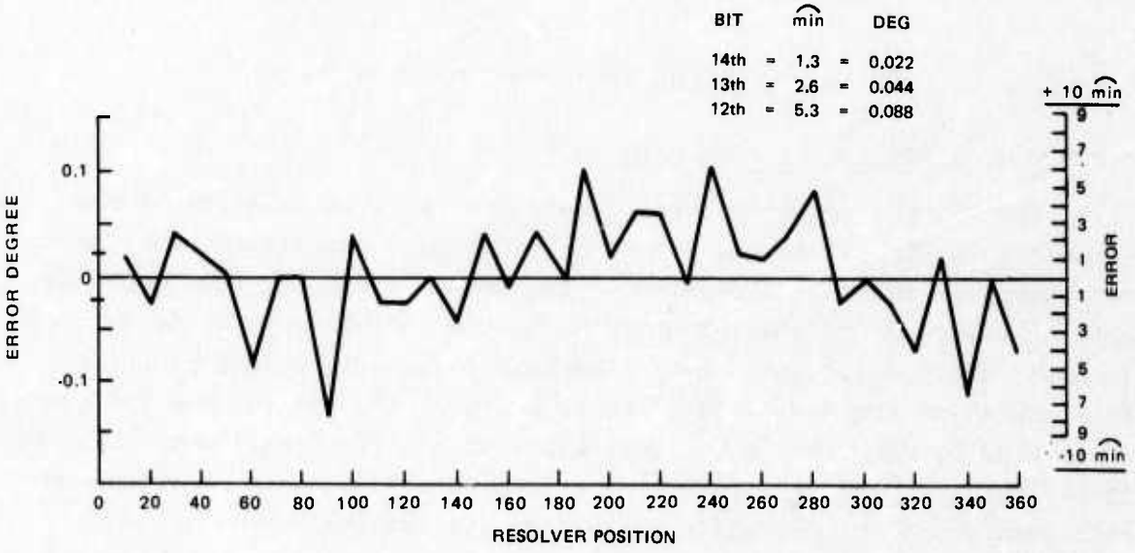


Figure 4-6. R/D converter error at 30°C.

4.4 Future Extended-Resolution Investigation

Future areas of investigation that may prove fruitful are mentioned in the following. These ideas are intended to overcome limitations and resolve problems that are well known or have appeared during this investigation.

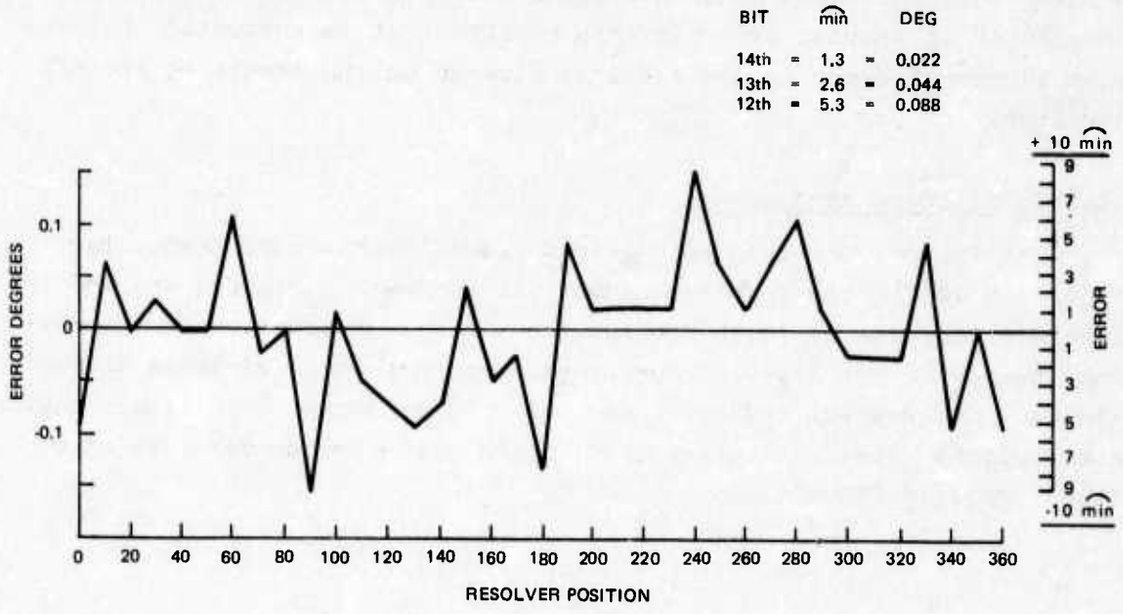


Figure 4-7. R/D converter error at 90°C.

4.4.1 Redistribution of Loop Gain

The PLL R/D converter should have the gains of portions of the circuitry shifted in such a manner as to allow a significant intrinsic gain increase in the PSD portion of the loop. Possibly, this could be done by using an implementation of a "co-tan loc" PSD where the gain of this circuitry would increase as the loop is brought closer to null. This would involve additional circuit design. The gain of the VCO can be lowered to make this functional block of the PLL less susceptible to LPF output noise and jitter. A crystal stabilized VCO is recommended as a stable and intrinsically noise-free element worth investigating. These two modifications would shift the gain of the PLL to the front end in an attempt to capture three more bits of resolution.

4.4.2 Future Extended-Temperature-Range Investigation

The usable temperature range of most commercial resolvers is quite limited, due to the copper-temperature coefficient. The resolver phase shift with temperature is on the order of 0.03 electrical degrees per degree Celsius. The phase-locked-loop phase shift is at least an order of magnitude better. Hence, a method of sensing the temperature of the

copper in the resolver and incrementing the phase of the PLL a corresponding amount should be investigated and developed. Such a resolver and readout unit would be extremely attractive in terms of cost and design simplicity.

4.4.3 Strobe-Generator Investigation

The strobe used to read the phase data contained in the PLL is now available from the crystal-controlled clock used to generate the timing waveforms. To make a PLL R/D converter stand alone, without additional circuitry, an internal strobe generator must be implemented. This could be derived from the resolver-excitation-frequency sinewave using a simple phase-locked loop to generate a squarewave strobe. A temperature-compensated strobe from an auxiliary resolver winding is also a good possibility.

4.5 Electronic Design Considerations

4.5.1 Bode Analysis

The composite Bode diagram of the R/D phase-locked-loop converter shown in Figure 4-8 was made by plotting the responses of the individual functional portions of the circuit from Figure 4-8, and then summing for the result.

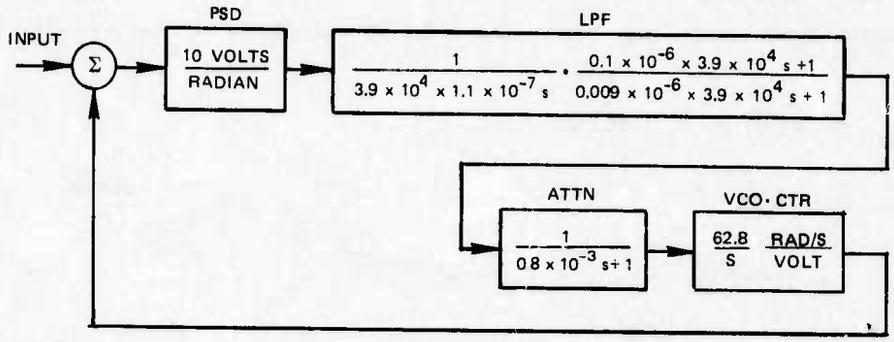


Figure 4-8. Block diagram of PLL with Bode gains.

The LPF response containing a lead-lag network is chosen to ensure stable PLL operation. One additional lag network is employed between the LPF output and the VCO and causes the slope of the loop-gain plot in Figure 4-9 to have a slope of -3 instead of -2 at high frequencies. The open-loop phase plot indicates an adequate margin of stability.

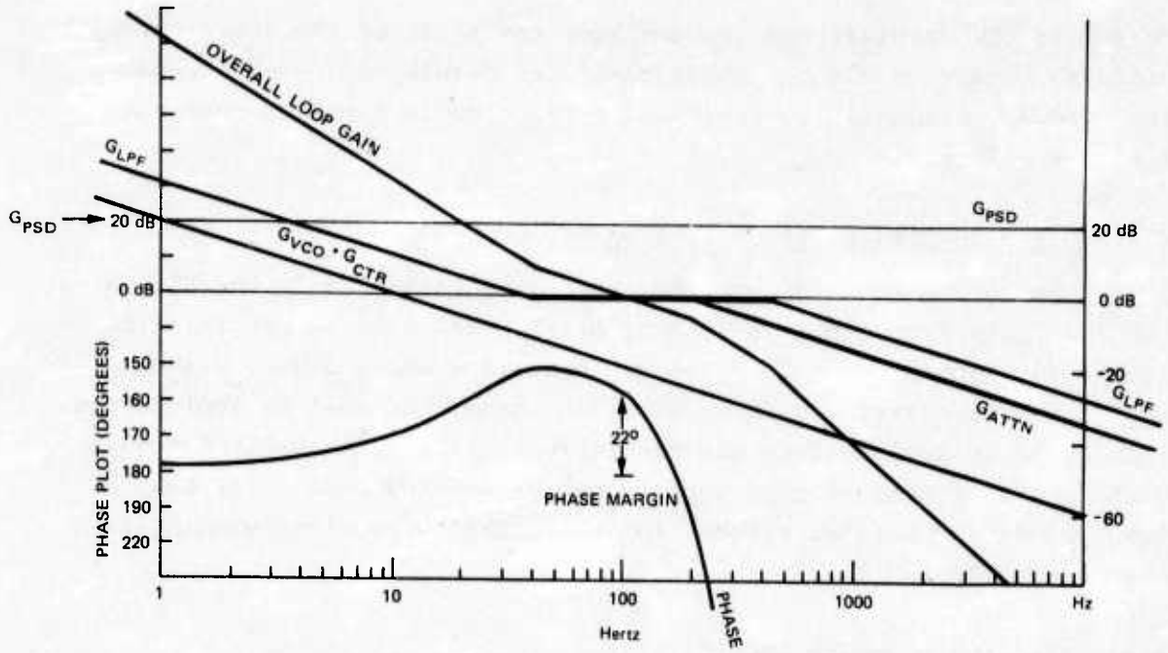


Figure 4-9. Bode plot of R/D converter.

4.5.2 Phase-Sensitive Detector

The phase-sensitive detector (PSD) generates an analog error signal, ε, that is proportional to $\sin(\phi - \theta)$ (see Figure 4-10). In its elementary form, the PSD block multiplies the input sinusoid by a feedback squarewave from the loop counter. The average value is calculated as

$$V_{PSD} = \sin(\omega t + \phi)[s(\omega t + \theta]$$

$$V_{PSD} = [\sin \omega t + \phi][\cos(\omega t + \theta) + \text{higher odd harmonics}]$$

$$V_{PSD} = \frac{1}{2} \sin(\phi - \theta) + \text{even harmonics}$$

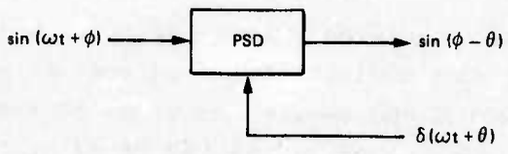


Figure 4-10. Phase-sensitive detector block diagram.

The PSD that was used in our demonstration R/D converter has an additional feedback waveform of $s(\omega t + \theta + \pi/2)$ that also produces the error signal $\frac{1}{2}\sin(\phi - \theta)$. This is summed with the other error signal at the input of the low-pass filter to produce $\sin(\theta - \phi)$. Figure 4-11 shows the Hypha converter in its primary form.[1] The higher-order harmonics produced by squarewave feedback, however, are a detriment to the overall accuracy of the circuit, since they cause ripple in the LPF output.

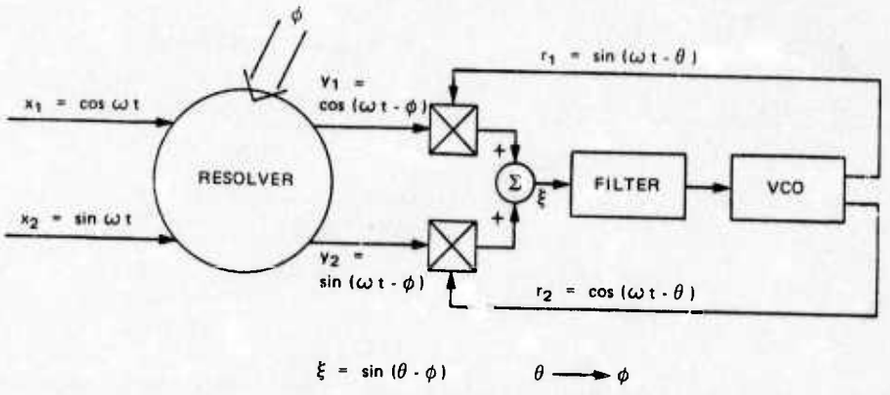


Figure 4-11. R/D converter block diagram.

It is the ripple voltage at LPF output which contributes directly to the phase error in the output data. To filter the ripple, an RC filter network is usually added to practical PLLs. Additional ripple minimization can be achieved by feeding back a signal that more closely resembles a sinusoidal waveform. The object here is to eliminate, or reduce in amplitude, the higher-order squarewave harmonics.

To approximate a sinusoidal signal, the pedestal waveform shown in Figure 4-12 is used. This waveform consists of steps which are evenly spaced, and which have amplitudes that are weighted with a sinusoidal function. The general relationship between the number of steps and the retained harmonics is

$$\text{Harmonic number} = \sum_{M=1}^{\infty} MN \pm 1$$

where M includes all positive integers and N is the number of steps. Thus, a 12-step wave contains the 11th, 13th, 23rd, 25th, and succeeding

harmonics, and the amplitude of each retained harmonic is inversely proportional to the number of harmonics—the same relationship as that of the squarewave. Pedestal weighting of the squarewave feedback to approximate a sinusoid has been costly, in terms of parts count in most schemes, especially in a double-input PLL.

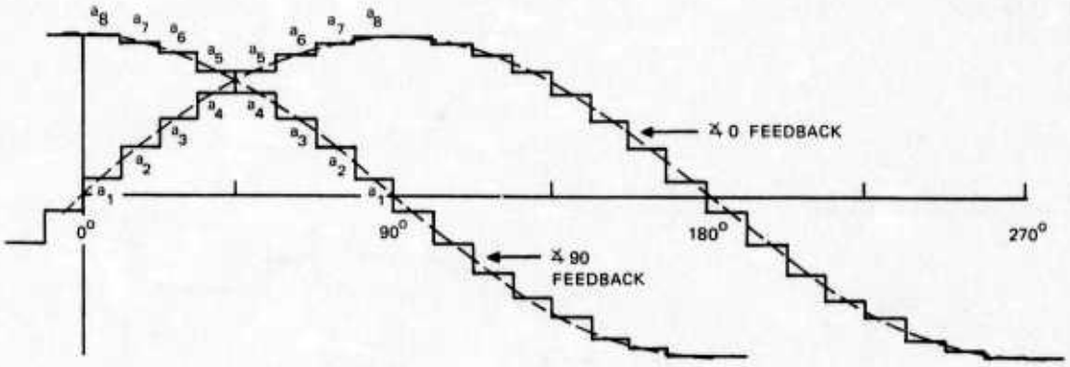


Figure 4-12. Effective-pedestal-feedback sine and cosine waveforms.

Standard pedestal-weighting approaches only partially take advantage of the symmetry present in the sinewave-feedback waveforms. Moreover, one switch is usually used for each independent weight required. This approach detailed in the following takes full advantage of sinewave symmetry and available switch states.

Sample feedback waveforms for a double-input PLL are shown in Figure 4-12 for a 32-step pedestal waveform (eight samples per quarter cycle). At the worst, this pedestal was realized with 16 switches and 16 resistors and, at best, with 8 resistors, but still with 16 switches.

There is another degree of symmetry in the two waveforms of Figure 4-12, which permits multiplexing values a_5 through a_8 with a_1 through a_4. That is, values a_5 through a_8 can multiply one input waveform while values a_1 through a_4 multiply the other (see Figure 4-13).

The first DG191 switch and all four phases of the input signal are required in any scheme to effect the multiplication by negative numbers. The second DG191 is used to multiplex the two four-weight networks between the ∡0 input and the ∡90 input waveforms. The four weights can be accomplished economically as shown in Figure 4-14.

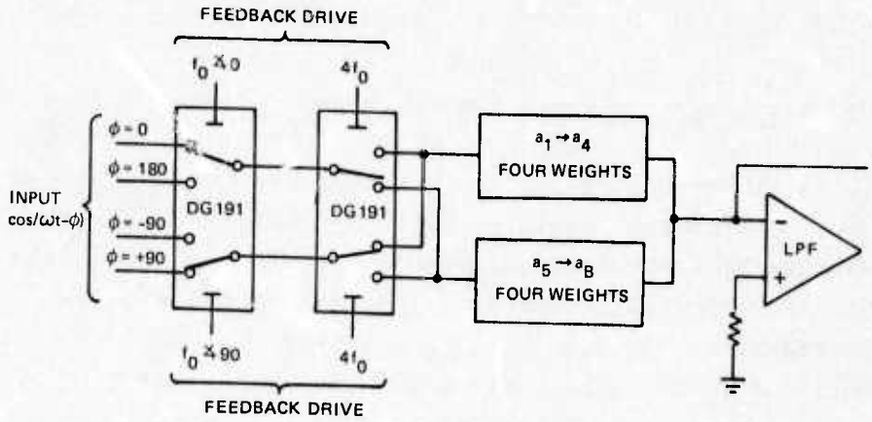


Figure 4-13. Switch diagram for pedestal-feedback PSD.

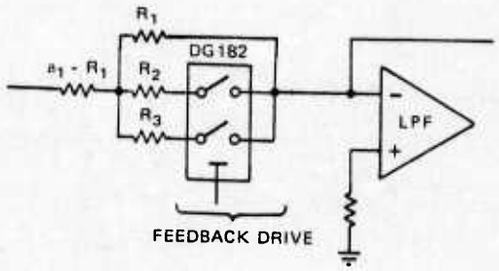


Figure 4-14. Basic diagram for resistor-value computation.

The values of resistors R_1 through R_3 must be solved in simultaneous equations to match them to weights a_1 through a_4 (or a_5 through a_8). These equations, without derivation are

$$\frac{1}{R_1} + \frac{1}{R_2} = \frac{1}{R_1 + b_1 - b_4} \qquad (4\text{-}1)$$

$$\frac{1}{R_1} + \frac{1}{R_3} = \frac{1}{R_1 + b_2 - b_4} \qquad (4\text{-}2)$$

$$\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} = \frac{1}{R_1 + b_3 - b_4} \qquad (4\text{-}3)$$

and solving for R_1

$$0 = -\frac{1}{R_1} + \frac{1}{R_1 + b_1 - b_4} + \frac{1}{R_1 + b_2 - b_4} - \frac{1}{R_1 + b_3 - b_4} \qquad (4\text{-}4)$$

In Eq. (4-1) through (4-4), the b values are proportional to the reciprocal of the sinewave values of Figure 4-12, ($b_n \propto \frac{1}{a_n}$). This is because resistors R_1 through R_3 are source resistors for the op amp LPF and, as such, are inversely proportional to gain. Equation (4-4) must be solved by iteration for R_1. With R_1 known, R_2 and R_3 follow easily from Eq. (4-1) and (4-2). The root of interest in Eq. (4-4) lies between (b_4 - b_3) and b_4, since other roots result in negative values of resistance.

This case has been solved to two significant figures, and the entire weighting configuration needed for a 32-step pedestal in a double-input PLL is shown in Figure 4-15.

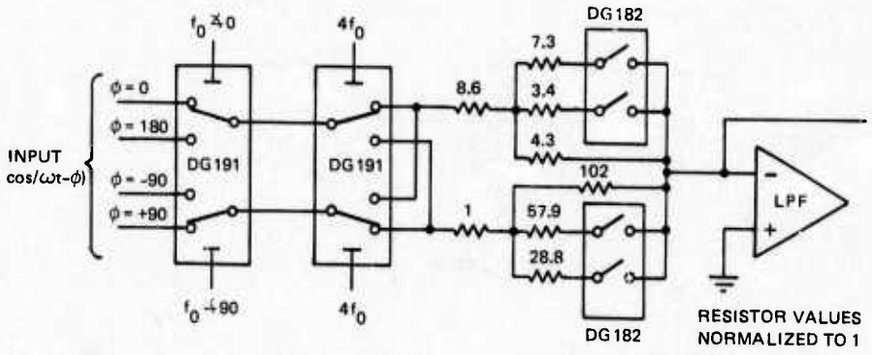


Figure 4-15. Normalized resistor values for pedestal PSD.

This approach provides two 32-step pedestals using two DG191s, two DG192s, and eight resistors. The feedback waveforms needed to drive the switches are simple countdown frequencies, or EX-ORs of countdown frequencies, and no complex decoding is required.

The simplicity of the approach is further apparent when the case of 16-step and 8-step feedback pedestals is investigated (see Figures 4-16 and 4-17). In these cases, the calculation of resistor values is simple and straightforward.

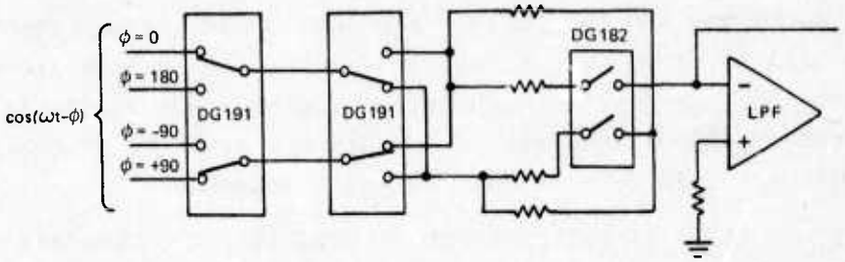


Figure 4-16. Two 16-step pedestals.

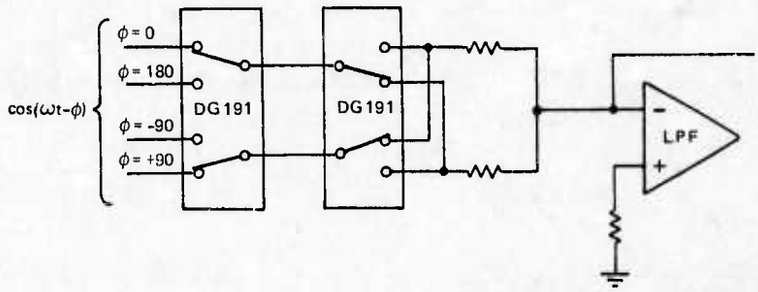


Figure 4-17. Two 8-step pedestals.

As one final example, suppose a 16-step pedestal was desired in a single-input PLL. The configuration would appear as shown in Figure 4-18.

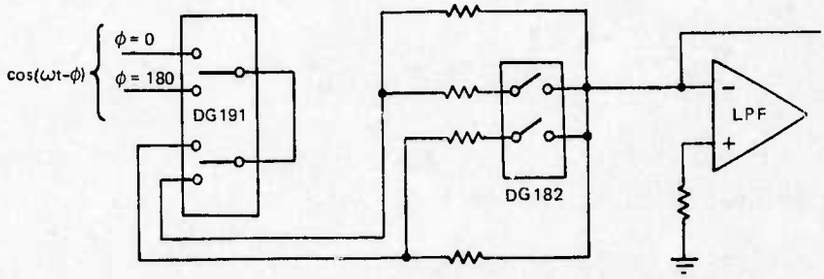


Figure 4-18. Single 16-step pedestal.

This technique results in such a reduction in circuit complexity that it is hard to argue against using a simple pedestal in any phase-locked loop. For example, an eight-step pedestal in a single-input loop requires one DG191 and two resistors where one half of the DG191 and one resistor would be required without a pedestal.

The gain of the phase-sensitive detector for the purposes of computing a Bode response can be calculated. The input sinusoid is a 10-volt peak and the multiplying waveform is scaled to a 1-volt peak. Multiplying these sinusoids yields

$$V_{PSD} = 10 \sin(\omega t + \phi) \times 1 \sin(\omega t + \theta)$$

$$V_{PSD} = \frac{10}{2} \sin(\phi - \theta)$$

$$V_{PSD} \doteq 5(\phi - \theta) \text{ for small angles}$$

Since this is a double-input phase-locked loop with both sine and cosine inputs, the gain of the PSD is doubled. Therefore,

$$K_{PSD} = 10 \text{ V/rad}$$

4.5.3 Low-Pass Filter

All harmonics in the input of the voltage-controlled oscillator, except for dc components, will give rise to a synchronous periodic modulation of the output phase and, hence, will distort the digital output signal. The error will appear as a nonlinearity if the strobing is synchronous and can be cancelled out, to a large extent, by careful functional and electrical design.

The LPF response contains a lead-lag network to ensure stable operation of the PLL. The LPF consists of an operational amplifier and a resistor/capacitor network in its feedback loop (see Figure 4-19).

$$K_{LPF}(s) = \frac{1}{sR_1(C_1+C_0)} \cdot \frac{sR_0C_1 + 1}{sR_0C_{eq} + 1}$$

where

$C_0 = 0.01\ \mu F$ $\quad R_0 = 39\ k$

$C_1 = 0.1\ \mu F$ $\quad R_1 = 39\ k$

$C_{eq} = C_0 \parallel C_1 = 0.009\ \mu F$

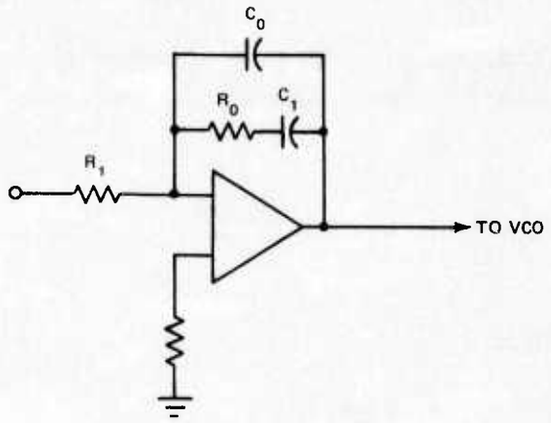


Figure 4-19. Low-pass filter.

Resistors R_0 and R_1 have the same value, which locates the midband section of the Bode plot of the LPF at a gain of 1. The lead breakpoint is located by R_0 and C_1 at 40 Hz. The lag is established by the parallel combination of C_0 and C_1 breaking with R_0, and was chosen to be 450 Hz. Finally, the low-frequency 1/s portion of the LPF was located at 35 Hz, using input resistor R_1, breaking with the sum of C_1 and C_0. The composite transfer function is

$$K_{LPF}(s) = \frac{1}{3.9 \times 10^4 \times 1.1 \times 10^{-7}\ s} \cdot \frac{0.1 \times 10^{-6} \times 3.9 \times 10^4\ s + 1}{0.009 \times 10^{-6} \times 3.9 \times 10^4\ s + 1}$$

4.5.4 Attenuator Section

The RC filter section is put in the loop to provide additional filtering of the higher-order harmonics of phase detection; the break was chosen to be at 200 Hz.

$$\frac{1}{Ts + 1} = \frac{1}{0.8 \times 10^{-3}\ s + 1}$$

where

$$T = \frac{1}{2\pi(200\ Hz)}$$

4.5.5 Voltage-Controlled Oscillator

The VCO output frequency is proportional to its input error voltage. The VCO phase, which is the integral of its frequency, is proportional to voltage multiplied by the duration of the input error signal. The lower harmonic frequencies at the output of the PSD are attenuated least by the

PLL low-pass filter and, hence, cause the largest phase deviations. For the case of the 400-Hz ripple frequency, the phase error is given by

$$\phi_e = V_e \frac{K_{VCO}}{s}$$

where

V_e = error voltage

ϕ_e = phase error in radians

K_{VCO} = VCO and counter gain in rad/s/V = 2.5% ω_0

ω_0 = $2\pi f_0$

The VCO center frequency of 52 MHz was chosen to yield 17 bits and still retain a fundamental loop frequency (f_0) of 400 Hz.

The VCO chosen to be used in this R/D converter is the 74S124 Schottky voltage-controlled oscillator from Texas Instruments. The center frequency is established by a single external capacitor as

$$f_c = \frac{500}{C_{ext}}$$

where

f_c = center frequency in MHz

and

C_{ext} = external capacitance in pF

There are two voltage-sensitive inputs on this device, one setting the frequency range (i.e., the gain constant, K_{VCO}), and one setting the frequency control. The output is compatible with Schottky clamped TTL logic. The main advantages of this device are frequency stability, high frequency operation, and ease of interface with logic.

4.5.6 The Countdown Chain

In the phase-locked-loop R/D converter, the VCO drives a synchronous counter. This counter contains the phase information which can be read by, and stored in, bi-stable latches.

The counter divides the VCO frequency by 2^{17} in the subject R/D converter. The counter recycles once every 400 Hz. Strobing occurs at the beginning of every cycle to sample output phase, θ. The major problem with synchronous counters is that they require a certain minimum set-up time at each stage. At high frequencies these set-up times are not met because of propagation delays through previous stages. In this case, the VCO is running extremely fast for standard TTL logic and Schottky logic must be used for at least the high-frequency portions of the synchronous countdown. The other problem that can become a factor, is that the strobe must lock the data into the latches before the transients caused by the strobe signal can affect the PLL.

A novel solution has been developed to implement a synchronous counter that overcomes these difficulties: The VCO output is buffered and inverted using two Schottky nand gates, and then used to clock a Schottky synchronous ÷4 counter. This counter has been implemented using Schottky flipflops to count and provide an output ripple clock at 13.2 MHz. The period of this waveform is 76 nanoseconds and is used as a clock input for a standard TTL synchronous counter. The ÷4 Schottky flipflops guarantee that the ripple-clock output is indeed synchronous with the VCO.

The synchronous strobe circuitry is activated on the rising edge of the input strobe signal. Upon receipt of this rising edge, the 16th and 17th bits at the output of the synchronous ÷4 Schottky counter are latched a half cycle from the last count. This permits adequate settling time on the last two bits.

At the time the 16th and 17th bits are latched, the state of the 13.2-MHz ripple clock (which controls the 15-bit synchronous counter) is sampled. If the ripple clock is low, it means that at least one-half period of 13.2 MHz has passed since the last count of the 15-bit synchronous counter. (The 15-bit counter counts on the positive edge of the ripple clock.) This is adequate settling and set-up time and, accordingly, the latches are closed immediately on the lower 15 bits before they can count again. If another count were permitted, the lower 15 bits would then be out of phase with the 16th and 17th bits.

If the ripple clock is high at the time the 16th and 17th bits are latched, this means that the lower 15 bits have changed less than one-half cycle of 13.2 MHz earlier. Accordingly, the circuitry waits until the ripple clock transfers low before holding the lower 15 bits. This permits enough set-up and settling time, while still preventing an extra count on the part of the 15-bit counter.

The important aspects of this design are that the data is locked within 19 nanoseconds of the input strobe, before the transient of switching gates and latch-output states can upset the phase information.

SECTION 5

THE INTERPOLATOR: A METHOD TO REDUCE QUANTIZATION ERRORS IN PULSE REBALANCE INSTRUMENTS

This section comprises the body of Draper Laboratory report P-128 by Robert C. Carson, Jr., which will be presented 14 to 16 May 1975 at the Seventh Biennial Guidance Test Symposium at Holloman Air Force Base, New Mexico.

1. INTRODUCTION

Inertial instruments often employ a pulse rebalance scheme called delta modulation (e.g., Binary, Ternary, or Pulse Width Modulation) that forms the basis of both a feedback control system and an information system. The control system uses the torque pulses to maintain the controlled element near null. The information system processes the torque pulses to provide a readout proportional to the instrument input or its first integral. The resolution of this sum is governed by (1) the torque amplitude and (2) the pulse rate. For certain applications it is desirable to increase the resolution (decrease the quantum size) and the approach normally taken is to reduce the torque amplitude and/or increase the pulse rate. However, the amount of alteration is limited and may result in degradation of instrument performance. These limits are usually determined by the instrument dynamics and the signal-to-noise ratio.

This paper presents an interpolation technique that has been used to improve the quantization obtained from a pulse rebalanced inertial instrument (irrespective of the torque rebalance scheme) without affecting its performance parameters. The interpolator described employs phase-locked loop techniques. A model of the instrument is incorporated within the phase locked loop and this model is used for comparing the predicted response of the nulled element to the rebalance torque with the actual response.

2. INSTRUMENT LOOP DYNAMICS

Ideally, the integral of the input to an integrating instrument is represented by the sum of the rebalance pulses plus the torqued element's position. Figure 1 illustrates

a typical torque-to-balance loop (delta modulator). An input torque causes the controlled element (i.e., pendulum, float, etc.) to rotate and the loop dynamics force the controlled element back to null. The following transfer function approximates the instrument dynamics

$$\frac{\theta_{out}(s)}{torque_{in}(s)} = \frac{1}{Cs\left(\frac{J}{C}s+1\right)} \qquad (2\text{-}1)$$

where

C = coefficient of damping

J = moment of inertia (nulled member)

J/C = time constant

The position of the nulled element is sampled and, depending upon its polarity, a torque pulse (plus or minus) of constant width (determined by the sampling frequency) and constant height (determined by the torquing electronics) is applied. The average rebalance torque will equal the average input torque.

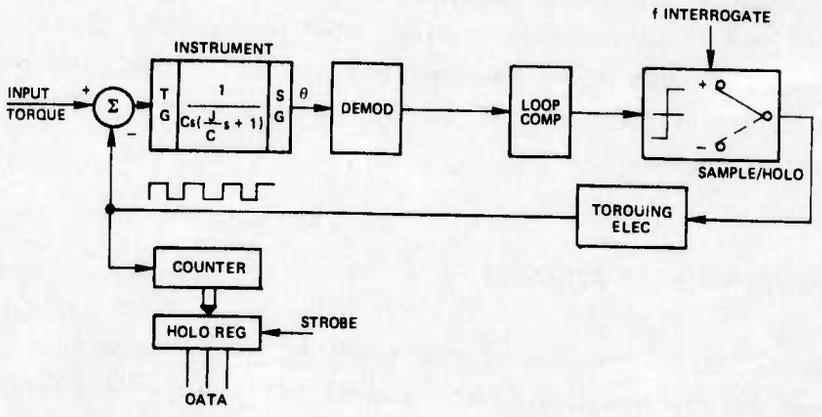


Figure 1. Binary Delta Modulator.

It is apparent that the torque-rebalance pattern would be +1, -1, +1, -1, etc., (1:1 moding) for zero input torque, and that for one-half maximum input it would be +1, +1, +1 -1, +1, +1, +1, -1, etc., (3:1 moding). The purpose of the loop compensation is to ensure that the rebalance torque is applied in single-pulse increments (i.e., zero torque cannot be 2:2 or 3:3, and one-half maximum input is 3:1 not 6:2 or 12:4). This guarantees a quantum size of one torque increment.

The net number of torque pulses (Figure 1), is counted and stored as a data sample. The height of the torque pulse is usually determined by the maximum rebalance torque required and the width by the interrogation frequency. For example, suppose we had an accelerometer rebalance loop with a 20-g scale factor and an interrogation frequency of 10 kHz; the quantization of such a loop would be

$$\text{Quantization} = \frac{\text{max. torque (scale factor)}}{f_{\text{interrogate}}} \tag{2-2}$$

$$= \frac{20\ g}{10\ kHz} = \frac{20 \times 32\ ft/s^2}{10^4\ pulse/s} \tag{2-3}$$

$$= 0.0644\ ft/s/pulse \tag{2-4}$$

$$\therefore \Delta\ \text{Velocity} = 0.0644\ ft/s = \text{one quantum} \tag{2-4}$$

The net rebalance torque can then be calculated using the following expression

$$\left[\frac{(\text{No. of plus pulses}) - (\text{No. of minus pulses})}{(\text{No. of plus pulses}) + (\text{No. of minus pulses})}\right]\left[\text{weighting of each pulse}\right] \qquad (2\text{-}5)$$

3. TECHNIQUES FOR INCREASING RESOLUTION

For certain applications, however, it may be desirable to increase the resolution (decrease the quantum size). Two methods for increasing resolution readily suggest themselves and should be considered. It is apparent from Figure 1, for example, that finer resolution could be obtained by increasing the interrogation frequency ($f_{interrogate}$). Alternatively, a pulse-width modulation scheme might be employed. These alternatives are briefly discussed below.

3.1 Increase $f_{interrogate}$

Increasing the interrogation frequency is one obvious means of achieving greater quantization. However, this technique may not be feasible because the delta modulator is an instrument-control system as well as an information system. That is, increasing the information rate directly affects the control performance and thus imposes physical limitations on the maximum rebalance rate. These limits are determined by instrument dynamics and signal-to-noise ratio. If the rebalance frequency is too high, the instrument will not respond sufficiently to each torque pulse and it becomes impossible to guarantee 1:1 moding. Also, to provide a given level of torque stability, the uncertainty of the width of

a torque pulse must be decreased in direct proportion to the torquing frequency. At high rebalance frequencies, variations in the nanosecond region may cause large variations in torque uncertainty.

3.2 Pulse-Width Modulation

A second technique to improve quantization is pulse-width modulation. This method forces the element to oscillate at a predetermined frequency and changes the ratio of plus-to-minus torquing at set increments within the period of oscillation, as shown in Figure 2. This technique has merit in that it somewhat isolates the control and information requirements. However, an area of concern is again the minimum torque increment. Can the timing be made stable enough and can the torque (through instrument mechanisms) be made linear enough throughout the entire torque range? In certain practical applications, this method can decrease static quantization by a factor of 4 to 8 over a conventional binary or ternary delta modulator.

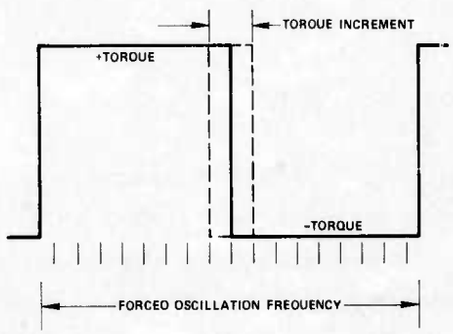


Figure 2. Pulse-Width Modulation.

4. THE INTERPOLATOR TECHNIQUE

Figure 3 shows the concept of integrating a typical delta modulator with an interpolator. This scheme separates the rebalance (control) loop from the information system. The advantage of the interpolator over the other methods described is based on creating a model of the instrument and comparing how the instrument should respond to the rebalance torque versus how it actually responded. Within the limitations imposed by the accuracy of the model, the output of this comparison is, in fact, proportional to the difference between the input torque and the rebalance torque. If the rebalance torque exactly equals the input torque, θ_{model} and θ_{actual} will cancel. However, if θ_{actual} differs from θ_{model}, an error signal will be generated that is proportional to the uncompensated input torque. Using the interpolator technique, the error signal changes the frequency of the VCO. The sensitivity of the VCO is such that it will add or subtract 2^n pulses for the equivalent motion of one torque increment. The overflow of the n^{th} bit in the up/down counter in the phase-locked loop represents the net applied torque pulses, and the lower bits indicate fractional torque pulses.

5. PRINCIPLE OF OPERATION

The interpolator (Figure 3) employs a phase-locked loop that is used as a digital low-pass filter as well as an A/D converter. There are three inputs to the loop: the VCO reference frequency, $S(\omega t)$, which is selectable and determines the center frequency of the VCO; the torque word, which controls the rebalance torque to the instrument; and

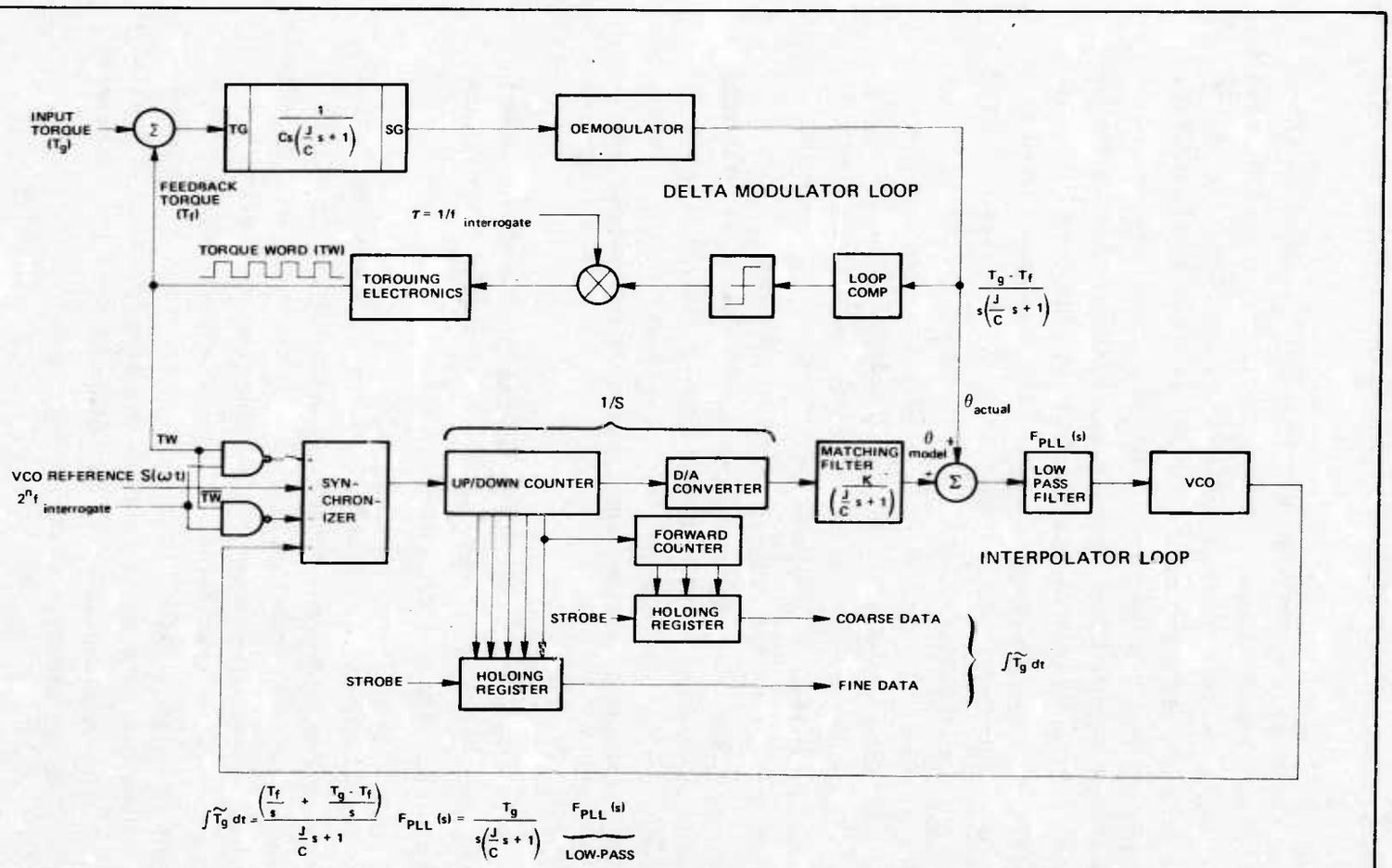
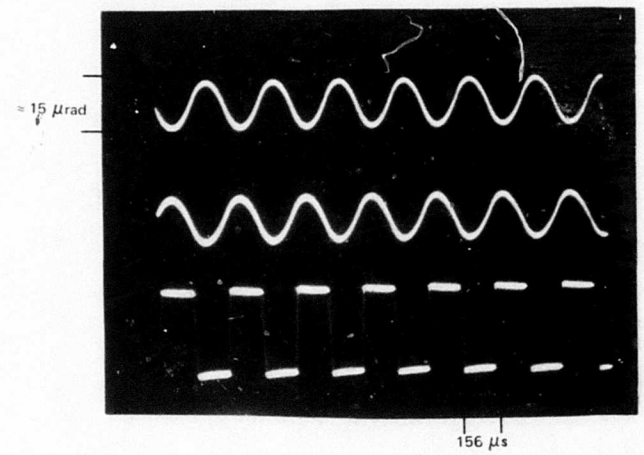


Figure 3. Delta Modulator with Interpolator, Functional Block Diagram

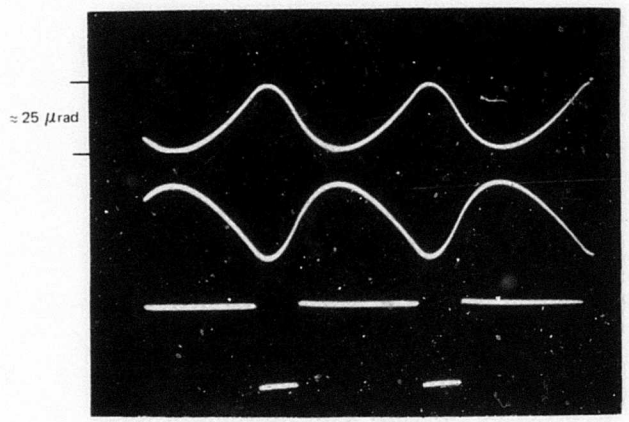
θ_{actual}, which is the response of the nulled element to the rebalance and input torque. For each positive (negative) torque pulse (TW), 2^n pulses are uniformly added (subtracted) in the up/down counter and, in turn, clocked into the D/A converter. The output of the D/A converter represents the integral of the rebalance torque (open loop, i.e., without the VCO feedback frequency). The output of the matching filter is an indication of how the controlled element should have responded to the rebalance torque (TW). This signal (θ_{model}) is thus compared with θ_{actual} and filtered. The difference is therefore an estimate of the input torque. The output frequency of the VCO thus is proportional to the input torque. The VCO will add (subtract) exactly 2^n pulses for the equivalent error of one torque pulse to maintain the input to the low-pass filter at null when the loop is closed. Thus, θ_{model} approximates the instrument's response to both the instrument's rebalance torque and to the input torque. Figure 4 shows waveforms of the feedback torque, θ_{model}, and θ_{actual} for zero, and one-half, the maximum input torque, respectively.

Data can be accumulated by either counting the output frequency of the VCO directly or strobing the up/down counter to obtain the integral of $T_g dt$.

The material in Figure 5 illustrates how an approximation of the bandwidth and frequency characteristics of the interpolator can be calculated. As can be seen from the example, bandwidth and loop response can be selected by varying the loop gain and low-pass filter characteristics. It is also apparent from this figure that if τ_{LPF} is small as compared to τ_f then the data obtained from the interpolator is available at the same bandwidth as would be obtained from the instrument above but at an improved quantization level.



(A) INPUT TORQUE (ZERO)



(B) INPUT TORQUE (½ MAX)

Figure 4. Interpolator Waveforms

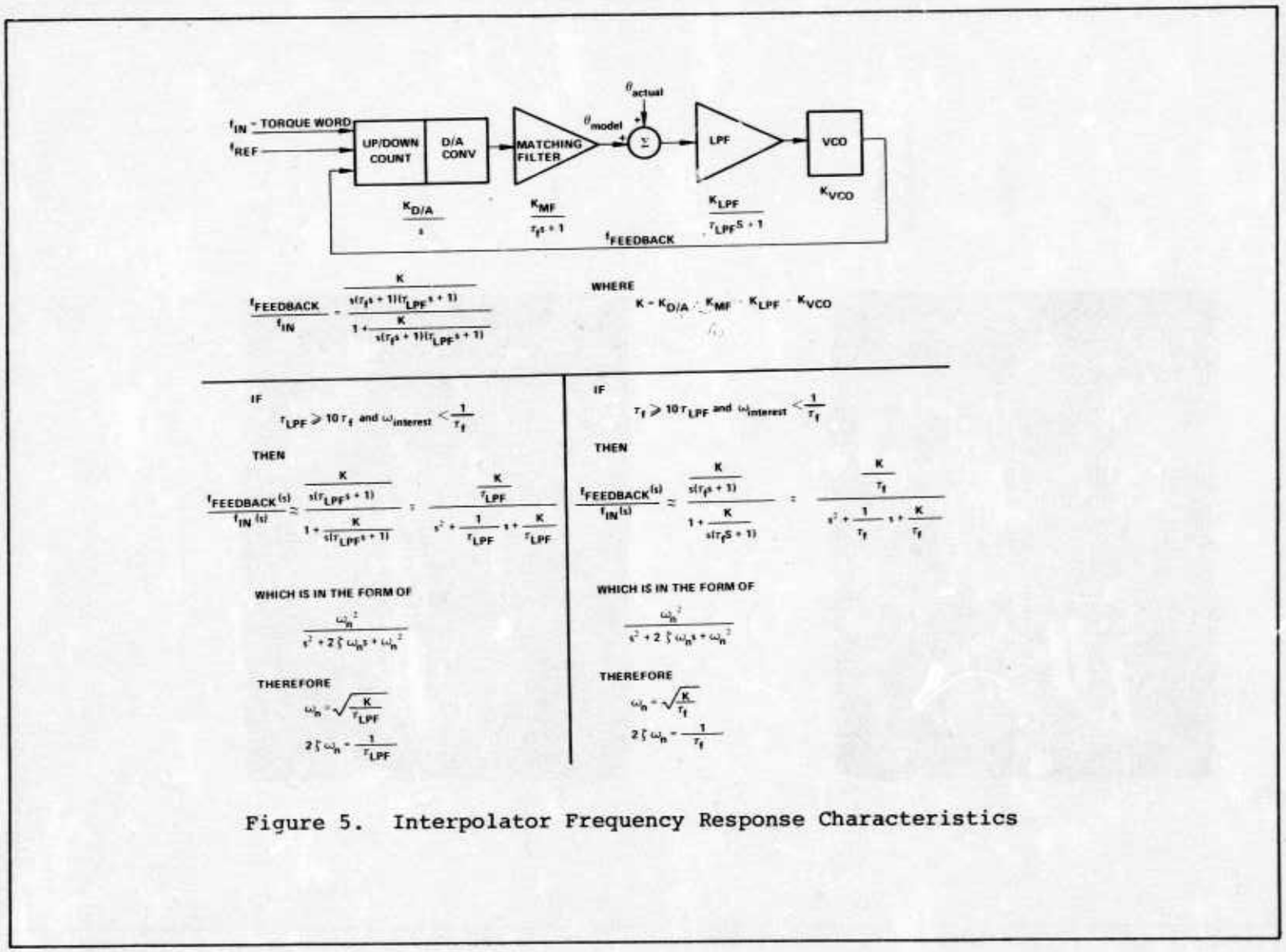


Figure 5. Interpolator Frequency Response Characteristics

6 . PROTOTYPE TESTING

To demonstrate its feasibility, a prototype interpolator was integrated with a pulsed integrating pendulous accelerometer and its associated binary torque-to-balance loop. The interrogate frequency of the delta modulator was 6.4 kHz. Higher rebalance frequencies would be impractical because of instrument dynamics. The interpolator was designed to yield a factor-of-32 improvement in quantization.

An experiment was set up so that data from both the binary delta modulator and the interpolator could be recorded simultaneously. Continuous data was accumulated by recording the output of the delta modulator and the interpolator at either 2.56- or 0.32-second intervals.

Using a computer, this data was reduced three ways to illustrate the effect of quantization:

(1) By employing a second-order moving-average technique where the average of the average of every 168 2.56-second data samples were plotted.

(2) By using a moving-average technique, as in (1), except that the slide and average were performed every two raw-data samples.

(3) By plotting each 0.32-second raw-data sample.

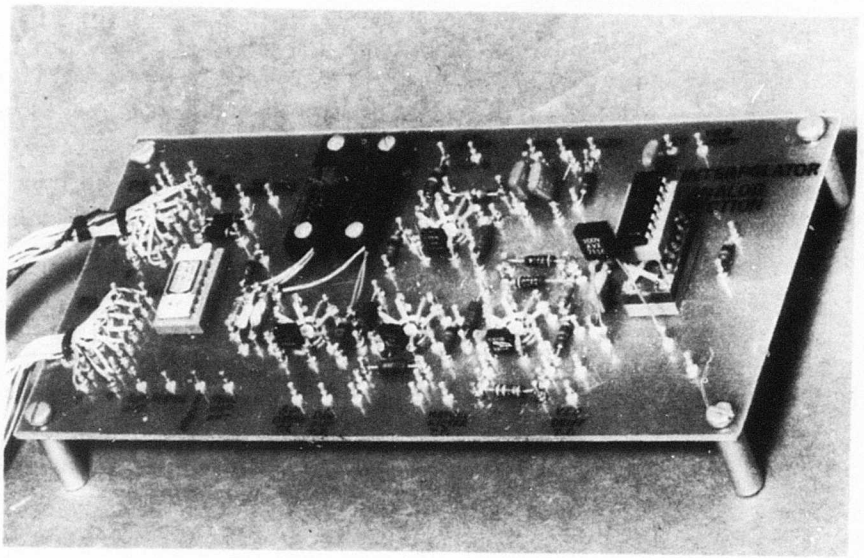


Figure 6. Interpolator Breadboard

Figures 7 through 12 are typical of the data obtained. Figure 7 shows typical results obtained with the delta-modulator while Figure 8 shows interpolator data. This data, collected over a 48-hour period, was processed by method (1).

The long averaging period was chosen so that the effect of quantization was well below deviations of the input acceleration during the averaging period. From these two figures it is obvious that at frequencies where quantization has been attenuated in both signals, the data obtained from the interpolator and delta modulator are indeed the same. Figures

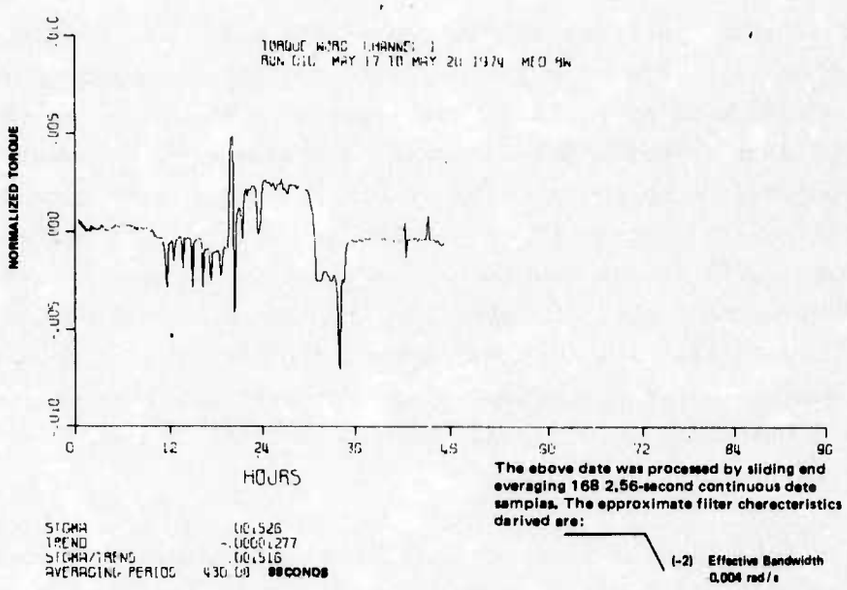


Figure 7. Delta Modulator Data Output (48 hr)

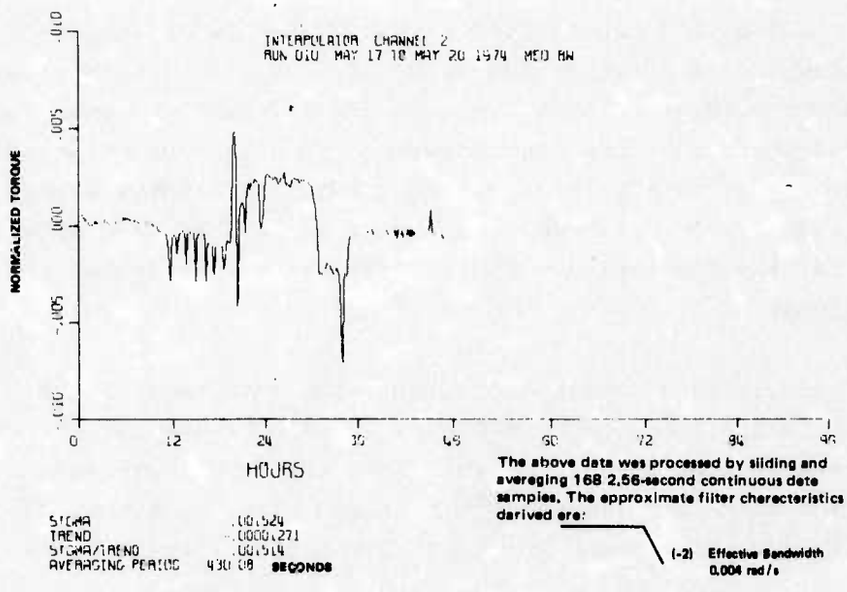


Figure 8. Interpolator Data Output (48 hr)

9 and 10 show the first 80 minutes of the same data reduced by method (2). Figure 9 is the delta-modulator output wherein the effect of quantization is apparent. Figure 10 is the interpolator output and illustrates a dramatic improvement in quantization at the same bandwidth. At this bandwidth (0.4 rad/s) the improvement in resolution is ≈ 12 as the delta-modulator data is not completely quantized. Figures 11 and 12 compare the delta modulator and interpolator by plotting 4 minutes of raw data that was accumulated every 0.32 seconds (the maximum input sampling time of data-acquisition system). At this bandwidth (6.85 rad/s) the improvement in quantization is ≈ 20.

Using techniques described in the reference* the power spectral density function (PSD) of the torque word data was computed and is displayed in Figure 13.

Inspection reveals two frequency ranges of interest. For frequencies greater than about 10^{-2} Hz, the PSD increases proportional to f^2 (+ 2 slope on log-log paper). This is a manifestation of the high frequency quantization noise which is clearly visible in Figure 9 as the signal assumes several quantized levels. However, for frequencies less than about 10^{-2} Hz, the PSD reflects the low-frequency information in the signal.

In terms of spectral content, the advantage of the interpolator is apparent in Figure 14 below where the PSD of the interpolator data is shown. Note that the low-frequency PSD is essentially the same in both PSD plots, but that the high frequency spectrum is quite different. This reflects

*William D.Koenigsberg, "Spectral Analysis of Random Signals-Techniques and Interpretation",CSDL Report E-2771, June 1973.

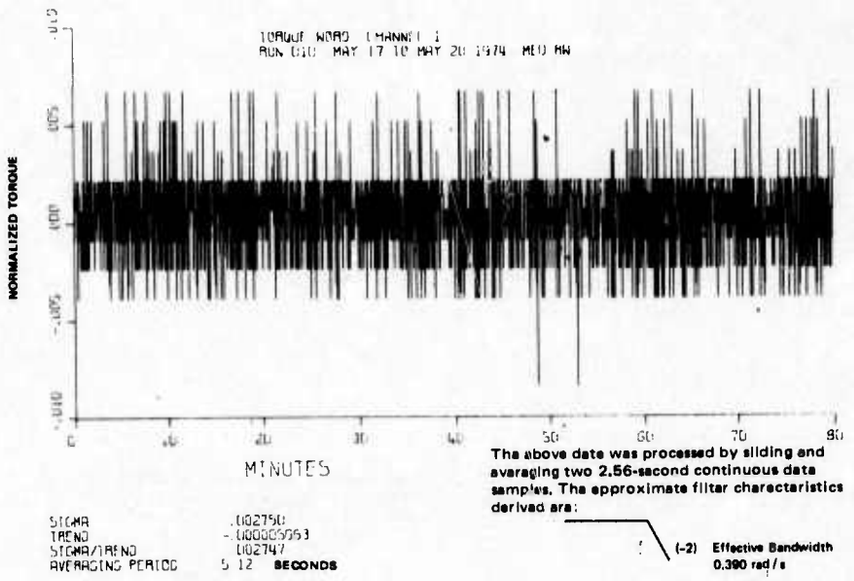


Figure 9. Delta Modulator Data Output (80 min)

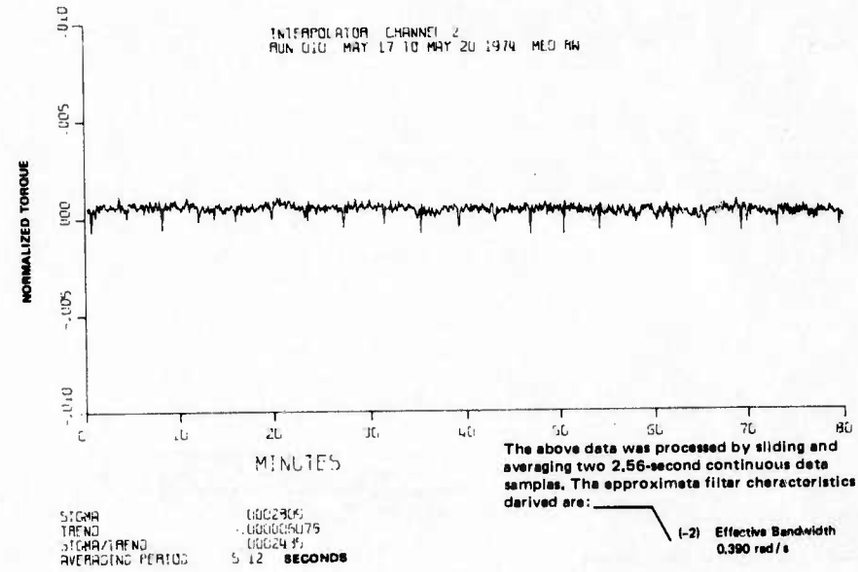


Figure 10. Interpolator Data Output (80 min)

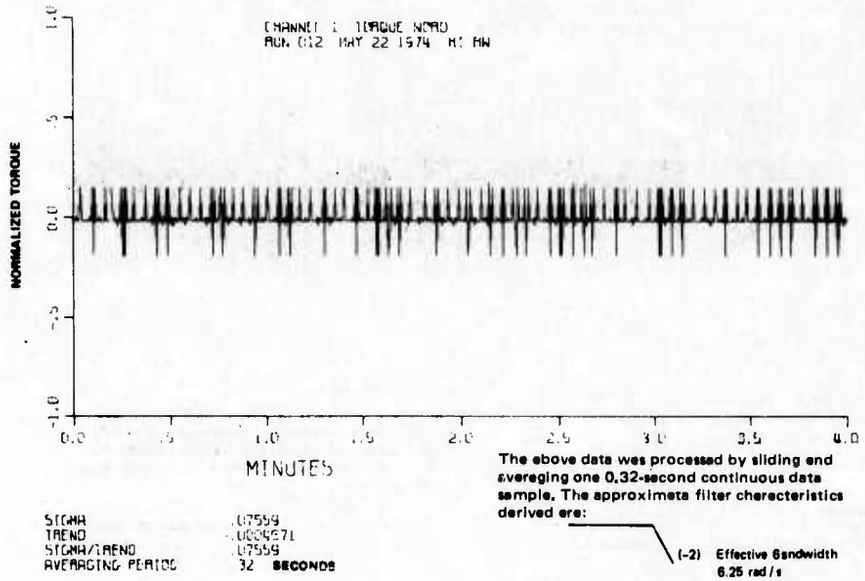


Figure 11. Delta Modulator Data Output (4.0 min)

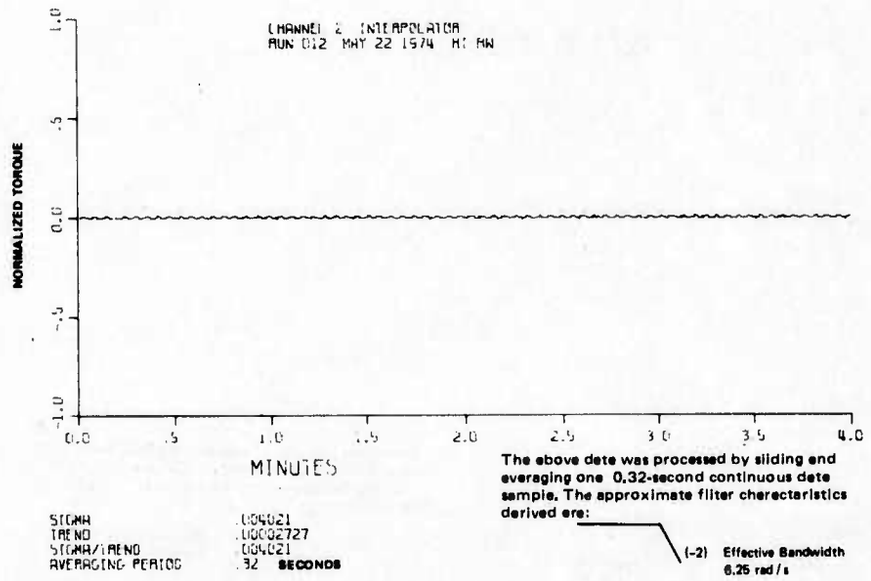


Figure 12. Interpolator Data Output (4.0 min)

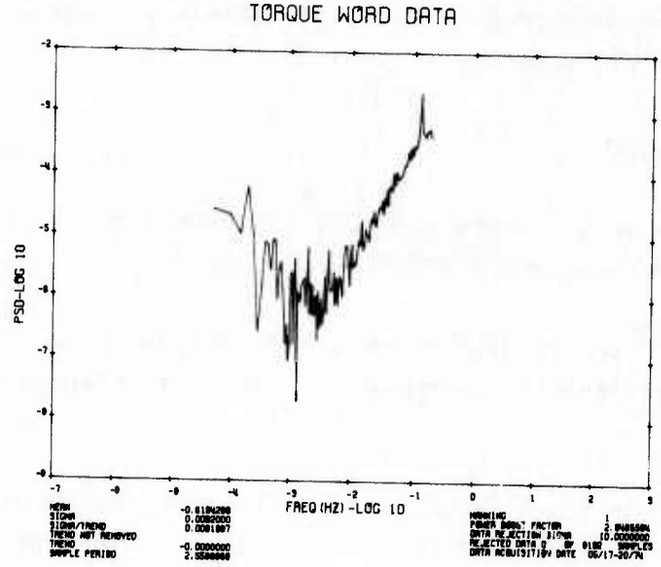


Figure 13. Power Spectral Density of Torque Word (Delta Modulator Data Output)

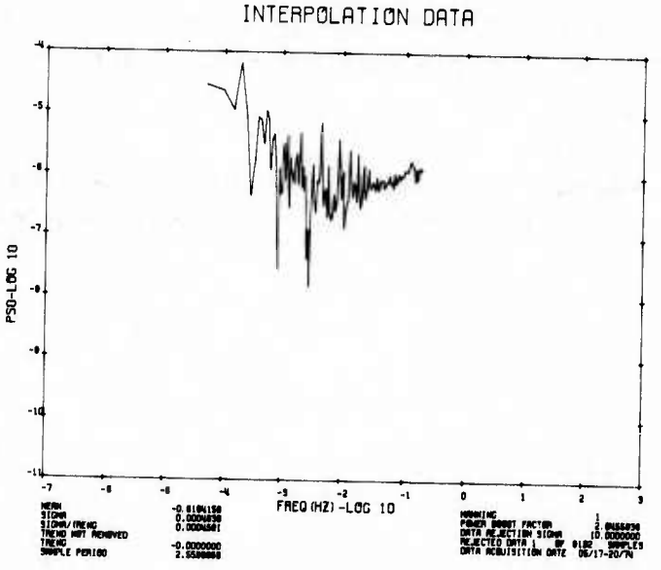


Figure 14. Power Spectral Density of Interpolator Data Output

the preservation of low frequency information as well as the suppression of the quantization noise.

7. CONCLUSIONS

This paper has described a method to reduce quantization errors in pulse rebalanced inertial instruments.

Based on the results to date, the interpolator technique has demonstrated the following advantages over other methods considered:

(1) Increased resolution without degrading other performance parameters. Problems associated with higher frequency torquing and narrower torque pulses are eliminated.

(2) Provides high-frequency filtering of noise. This is an inherent property of the phase-locked loop.

(3) Reduced complexity compared with other methods. This is a simple and easily implemented scheme.

SECTION 6

FEASIBILITY OF USING HYPHA TECHNOLOGY IN A UNIVERSAL SERVO LOOP

6.1 Introduction

The concept of a universal servo is illustrated in Figure 6-1. The phase-locked loop is the vital organ and is used for the following functions:

(1) To generate the necessary loop compensation.

(2) To provide high-frequency filtering.

(3) As an A/D converter to provide a fine error readout.

In order to investigate the feasibility of using Hypha technology in a universal servo two experiments were performed with an inertia wheel borrowed from another CSDL group. The purpose of these experiments was to verify the concept of employing phase-locked-loop techniques as the basic building block of either a delta modulator or positional servo-type loop. Again, some of the advantages of such a mechanization are thought to be that:

(1) The PLL provides a fine error readout (in digital form).

(2) It can be used to develop the necessary loop compensation.

For a positional servo this fine error, for example, would be the gyro output angle which in turn could be used for the compensation of kinematic coning. In a delta modulator, this fine error is proportional to the net difference between the feedback torque and the input torque, thus affording the advantages of the interpolator in that fine quantization is achieved without degrading other performance parameters.

The equipment consists of an inertia wheel with a one-speed resolver and torque motor mounted on its spin axis. Two experiments were run with this equipment to simulate both a pulse rebalanced accelerometer and platform gimbal. Figures 6-1 and 6-2 illustrate the mechanization of the accelerometer (delta modulator) and positional servo loops, respectively.

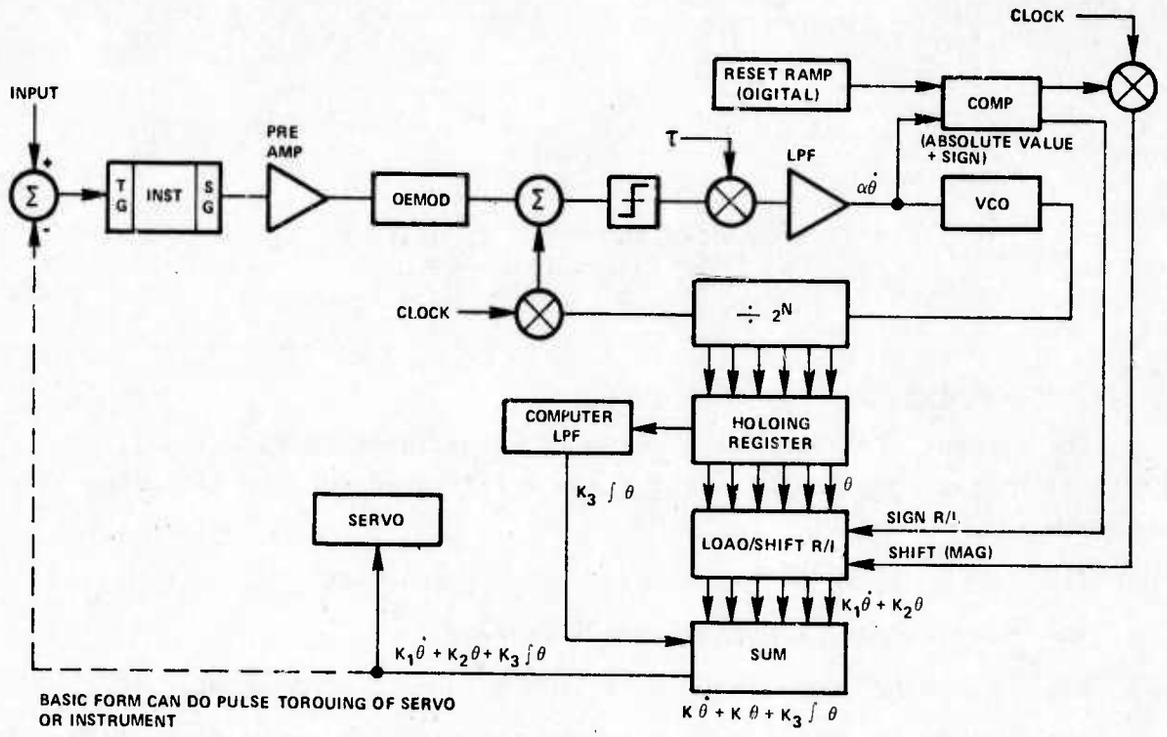


Figure 6-1. Universal servo.

6.2 Delta Modulator

Figure 6-2 illustrates how the inertia wheel was configured to simulate a pulse rebalanced accelerometer. The inertia of the wheel represents the inertia of the nulled element (float, pendulum, etc.). The resolver output is then analogous to the signal-generator output and the torque motor to that of the torquer within the instrument. The position of the nulled element (resolver output) is stored in phase of the 2^N counter in the phase-locked loop and, depending upon its polarity, a torque pulse of constant height and constant width is applied to drive it back to null. Ideally, the average input torque can be obtained by summing the net number of torque pulses plus the change in the nulled element's position. This affords the advantages of the interpolator concept in that quantization finer than 1 torque pulse is achieved without degrading other performance parameters.

6.3 Positional Servo

Figure 6-3 shows how the inertia wheel was used to mechanize a platform gimbal. An estimate of the gyro output angle is stored in the phase of the 2^N counter of the phase-locked loop. The input to the VCO

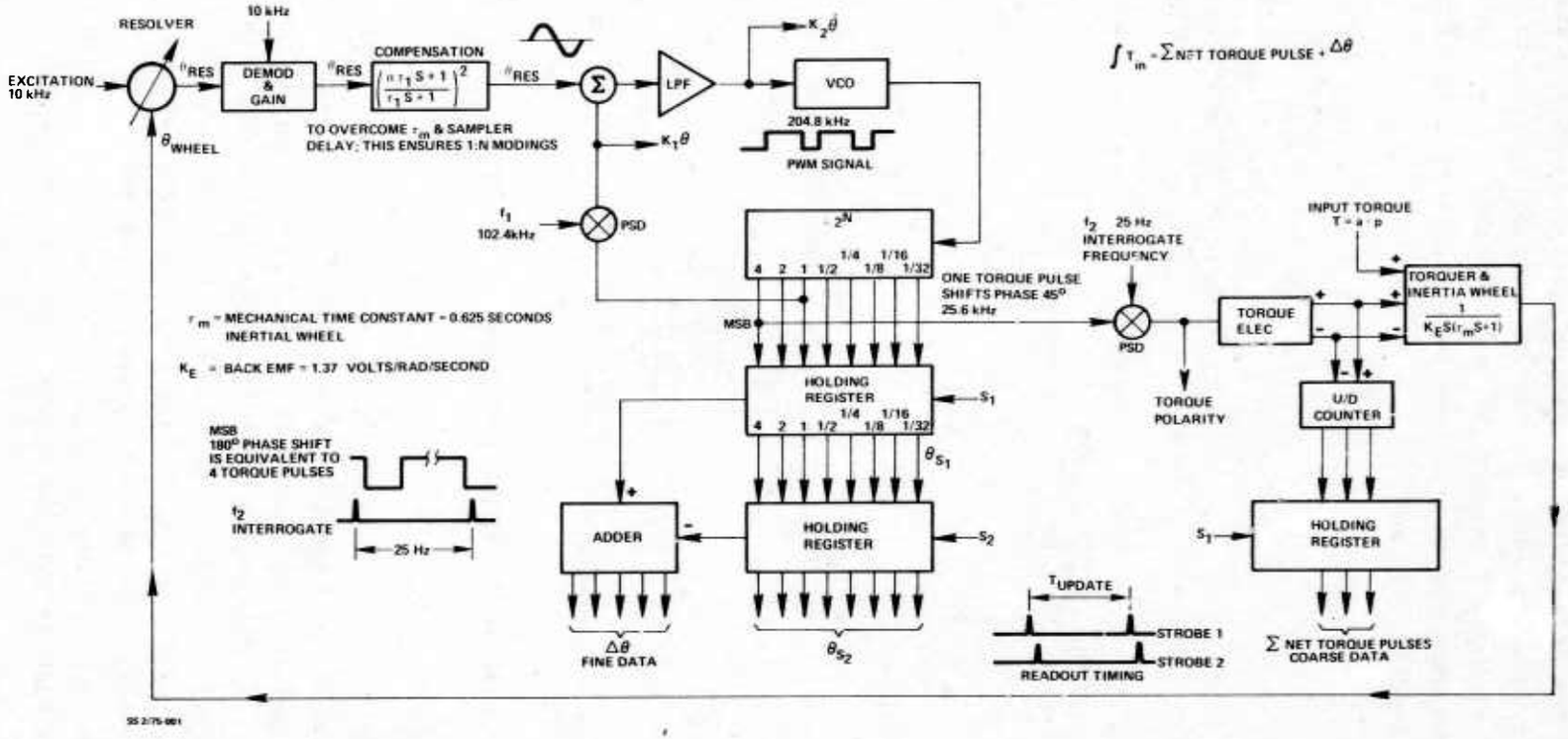


Figure 6-2. Universal-servo experiment—delta-modulator block diagram.

is an estimate of the derivative of position (i.e., inertial rate) and is summed with the position error to provide a lead function to cancel the effect of the platform's mechanical time constant. The fine position error could be used for such things as platform misalignment or compensation of kinematic coning.

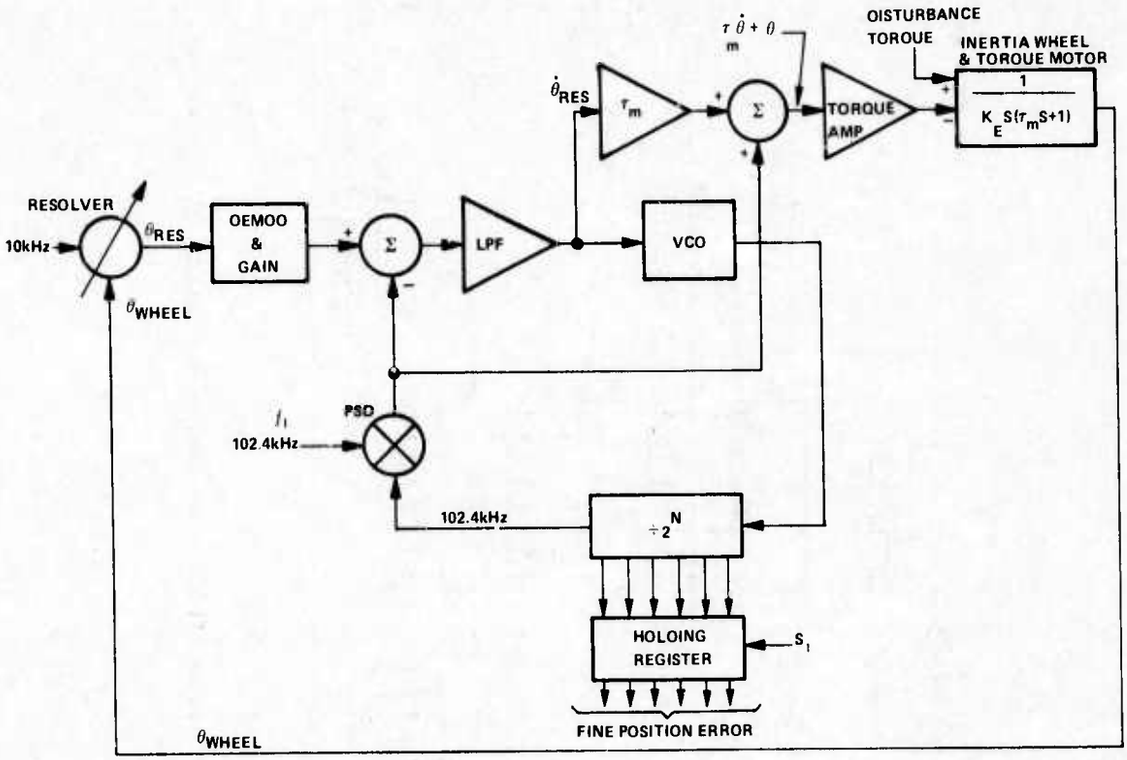


Figure 6-3. Universal-servo experiment—positional-servo block diagram.

6.4 Results and Conclusions

The concept of using a phase-locked loop as the heart of a universal servo has been verified by the experiments performed. Both loops were closed and performed as expected. In the accelerometer experiment, 1:N moding (see Subsection 5.2) and quantization equivalent to one thirty-second of a torque pulse was obtained. The positional servo closed and a fine error readout of less than 1 milliradian was observed. However, due to constraints imposed by the inertia wheel (low mechanical time constant and high bearing friction), further investigations are necessary. Areas such as dynamic errors, bandwidth considerations, and

noise immunity must be thoroughly analyzed before such a loop could be incorporated with an actual instrument or platform. Finally, it appears that the digital phase-locked loop described in Section 2 is well suited for such applications and would dramatically reduce the size and complexity of the circuitry.

PART C

MOTION COMPENSATION OF ADVANCED RADAR

by

George Schmidt

MOTION COMPENSATION OF ADVANCED RADAR

This is the Final Report under contract F33615-72-C-1335, Task 2.2, "Radar Inertial Systems." CSDL provided engineering support to the Electronically Agile Radar (EAR) Program Office during the period of performance of this contract. That support encompassed:

(1) Technical review of documentation prepared by various contractors and AFAL.

(2) Development of new analysis techniques for synthetic-aperture motion-compensation requirements and guidelines for EAR Phase-1 analyses.

(3) Development of B-1 environmental information for EAR.

(4) Interface between radar and inertial contractors.

(5) Special studies and support:

  (a) Pulse-rebalanced-accelerometer study.

  (b) Mounting study.

  (c) Doppler velocity study.

  (d) Aperture-weighting investigations.

  (e) Strapdown-sensor study.

  (f) Honeywell-modification-program support.

(6) Support at various design-review and technical-coordination meetings.

CSDL personnel technically reviewed and ranked all of the EAR contractors' Phase-Ø Final Reports. In addition, their Phase-1 proposals were also reviewed and ranked. CSDL also contributed to the AFAL Statement of Work and Subsystem Specification used in the RFP for Phase 1. Technical review of the EAR contractor was also performed. The Honeywell modification program for SPN/GEANS for EAR was also reviewed and CSDL continued to review progress reports on that program.

Throughout the period of this contract, CSDL worked closely with the MIT Electronic Systems Laboratory in an attempt to develop a unified method of evaluating the quality of radar displays subject to phase errors. The need for a unified approach became clear when it was necessary to compare and evaluate Phase-Ø contractors' work and previous criteria would not allow the comparison. The criterion subsequently developed considers clutter width, resolvable distance, flare ratio, peak side ratio, and main-lobe shift as the standard reference points for any SAR evaluation. This new criterion has been adopted by the EAR Program Office and will be applied to the EAR contractor.

CSDL continued its previous efforts to develop the B-1 environmental information necessary for EAR design. The efforts resulted in a complete environmental specification—air turbulence, etc.—available to the contractors at the start of the initial program. Further work in this area with NAR and Boeing has resulted in a final environmental specification pending actual flight-test data.

CSDL continued to function as an interface between radar contractors and inertial contractors; in a sense, translating their respective requirements to each other. The requirements for modifications to both the GEANS and LN-15S navigation systems for use in EAR were identified and presented to the Program Office.

During the course of providing the EAR program support, several critical problem areas were identified where CSDL had the capability to provide unique analyses. Each of the following items was investigated in detail and the results were forwarded to the EAR Program Office.

A special study on the use of binary rebalanced accelerometers in SAR motion compensation was begun when it was determined that previous analyses were incorrect. CSDL prepared an analytical prediction of expected performance and initiated detailed digital simulations for verification. The simulations were run at a very high integration rate so that instrument dynamics, electronics, and moding could be demonstrated. Various dynamic inputs such as ramp accelerations were generated. Different iteration rates to produce a phase-compensation signal were also introduced so that the effects of computation rates could be studied. From this study, it was concluded that a rebalanced accelerometer, properly mechanized, could be used for EAR if the quantization were between 0.0005 and 0.001 foot per second per bit.

A special feasibility study on the mounting of an EAR antenna and a SPN/GEANS navigator on the same base, but with the antenna in the radome area and GEANS in the forward avionics bay, was performed. Attention was given to the particularly severe B-1 vibration and shock environments. If such a common base could be vibration isolated from the aircraft, the wide-bandwidth requirements on the GEANS would be relaxed and no additional nuclear hardening would be required since the INS is still in the forward avionics bay. Such a solution was determined as feasible and the results forwarded to the radar contractor for consideration during Phase 1.

A unique aspect of the EAR is the multiple-position single-beam Doppler velocity-measurement capability. A special investigation was initiated to determine if contractors' claims were valid, particularly taking into consideration the pulsed operation of the radar as opposed to a conventional CW system. Effects of ground-terrain variations were also included in this study.

An investigation was performed to determine the effects of aperture-weighting functions on quadratic phase errors—the dominant type from inertial-motion sensing. It was determined that in order to maintain the same resolvable distance in the display, amplitude weighting actually tightens the requirements on quadratic phase errors because of the longer aperture times. One, of course, trades this off against improved integrated-side-lobe performance.

A separate Task 4 under this contract was initiated to determine the requirements for a separate motion-sensor package mounted on the antenna and mechanized in a master/slave configuration with SPN/GEANS. This study grew out of the identification of required mounting for the modified SPN/GEANS; if it cannot be mounted such that the EAR and GEANS are on the same base, separate antenna-mounted sensors will be required. The study involves determining the performance requirements for the inertial instruments, surveying available instruments and systems, designing the system to block-diagram level, detailing a program-and-fabrication plan, and implementing a detailed digital simulation of the complete B-1 environment, the inertial-sensor package, the motion-compensation mechanization, and the radar-display degradation. All milestones on this program have been met.

Consulting support to Honeywell has been provided for their attempts to use pulsewidth modulation or phase-locked loops to improve the GEANS accelerometer quantization. Monthly R&D status reports and program and test plans have been reviewed for AFAL, and CSDL personnel have attended design reviews.

The personnel allocated to Task 2.2 over this period have averaged one man per month.

PART D

EAR ANTENNA MOUNTED MOTION-COMPENSATION INVESTIGATION

by

George Schmidt

SECTION 1

INTRODUCTION

The overall objective of this investigation was to identify what existing motion-sensor instrumentation or combination of available sensors having a mature production base could be used to accomplish motion compensation for the Electronically Agile Radar (EAR). This 12-month technical effort has consisted of analysis, simulation, and preliminary design to block-diagram level in order to assess the technical feasibility and economic practicality of implementing a special-purpose motion-compensation sensor for EAR in the severe environmental conditions expected for strategic weapon system applications.

The results of this investigation are given in three separate volumes: Volume I summarizes the operational environment, the motion-compensation requirements, and identifies needed changes to available motion sensors. Volume II details a program plan for fabrication of an engineering demonstration and flight-test model of the recommended implementation. Volume III discusses the analysis and simulation techniques used to identify required motion-sensor performance for EAR and the resulting conclusions.

EAR is a multimode phased-array radar with all digital processing. The multiple functions include real beam ground mapping in the forward direction, synthetic-aperture (SAR) mapping to the side of the aircraft, terrain following, terrain avoidance, Doppler velocity measurement, and position-fix capability. It is presently being designed for low cost of ownership, for growth capability for air-to-air operations, and for improved SAR ground-map resolution.

The motion-compensation problem relates to the SAR mode, which is mechanized by transmitting radar pulses during an aperture length and properly digitally processing the radar returns over that time interval to create, in effect, an antenna length related to the distance traveled

by the aircraft during that interval. For high-speed aircraft, the synthetic antenna length can then be quite long and, hence, the ground-map resolution can be extremely small. Proper correction of the phase of each radar return is required to make a map; the phase is a direct function of the motion of the aircraft during that interval.

The Draper Laboratory effort has concentrated on determining the requirements for this short-term motion-measurement problem. A complementary AFAL/RWA effort has addressed the problem of integrating this motion sensor or slave system with a long-term precise master navigation system, which is physically displaced from the EAR-antenna-motion-sensor location. The AFAL effort is also addressing the use of inertial navigation-system update techniques using the EAR velocity and position-measurement capabilities. Volume III describes the integration of the master/slave studies with the motion-sensor studies and the resulting conclusions on required sensor performance.

SECTION 2

REQUIREMENTS AND ENVIRONMENT

EAR is being designed to meet future strategic weapon delivery requirements for aircraft such as the B-1, FB-111, or B-52. The motion-compensation requirements are intimately connected with the vehicle dynamic environment and throughout this report the B-1 environment during low-level penetration is taken as representative. This environment is listed in Tables 2-1 and 2-2.

The requirements for motion compensation in this environment, as developed in Volume III, are summarized in Table 2-3 for two cases of azimuth resolution in the SAR mode. The entries in Table 2-3 assume that there is:

(1) A 2g maneuver at a velocity of 600 feet per second at 50 nautical miles.

(2) A radar-squint angle of 20 degrees, with respect to the aircraft velocity vector.

(3) A turn rate of 20 degrees per second.

(4) The motion sensor mounted to the antenna which, in turn, is hard mounted to the aircraft.

(5) Hamming weighting being used.

(6) No other error source present.

For example, the maximum gyro drift specified assumes that no accelerometer bias is present.

Table 2-1. Maximum operational maneuvers.

Angular Motion	
Angle of attack	0 to + 9°
Angle-of-attack rate	± 20°/s
Angle of sideslip	± 5°
Angle-of-sideslip rate	± 20°/s
Flight-path angle	± 45°
Pitch angle	± 45°
Pitch rate	± 20°/s
Pitch acceleration	± 50°/s^2
Roll angle	± 90°
Roll rate	± 75°/s
Roll acceleration	± 150°/s^2
Yaw angle	Continuous
Yaw rate	± 20°/s
Yaw acceleration	± 30°/s^2
Linear Motion	
Longitudinal rate	2500 ft/s
Longitudinal acceleration	± 0.5 g
Lateral rate	βV
Lateral acceleration	± 1 g
Normal rate	α V
Normal acceleration	+3, -1 g or ± 2 g
Other	
Time at negative g	10 s

(Reference: B-1 Air Vehicle/Avionics ICD, Part 1, Functional and Reference Requirements, Rockwell International, April 1974, P. 80)

Table 2-2. B-1 random environment.

Turbulence Induced	Frequency Range
Vertical Load Factor	0 - 16 Hz
Lateral Load Factor	0 - 16 Hz
Pitch Rate	0 - 16 Hz
Yaw Rate	0 - 16 Hz
Roll Rate	0 - 16 Hz
Vertical Structural Deflection	0 - 16 Hz
Lateral Structural Deflection	0 - 16 Hz
Angular Deflection in Vertical Plane	0 - 16 Hz
Sinusoidal Vibrations	0 - 100 Hz
Random Vibration	0 - 2000 Hz
Terrain Following/Terrain Avoidance	
(Reference: Vol. III, Appendix A)	

Table 2-3. Maximum allowable individual error sources.

Illumination	Maximum Accelerometer Bias (μg) or Maximum Level Misalignment** (μrad)	Maximum** Gyro Drift (°/h)	Maximum*** Initial Velocity Error (ft/s)	Maximum**** Accelerometer Scale Factor Error (ppm)
Uniform	270 (1080)*	32.7 (261)	18.6 (74.6)	135 (540)
Parabolic	225 (900)	21.1 (169)	15.5 (61.9)	112 (450)
Cosine Squared	203 (812)	15.4 (123)	14.0 (55.7)	101 (406)
Hamming	196 (784)	16.5 (132)	13.5 (54.0)	98 (392)

*Table is for R = 300,000 ft, v = 600 ft/s, θ = 20°. Entries are for the growth resolution, entries in ( ) are for the design resolution.

**For an aircraft vertical maneuver, divide the entry by the number of maneuver g's plus one, for level misalignment or gyro drift.

***These maximum values are for motion compensation of the quadratic error. More stringent requirements exist for beam pointing and position-fix accuracies.

****For a 2-g maneuver.

For the case of a high quality IMU mounted directly on the antenna, the maximum individual error sources listed in Table 2-3 may be allotted among various contributors to give the specification listed in Table 2-4.

Table 2-4. Typical 1σ system specification.

Specification	Designed Resolution	Growth Resolution
Accelerometer		
Bias	196 μg	50 μg
Scale-Factor Error	98 ppm	25 ppm
3-dB Bandwidth	50 Hz	50 Hz
Quantization	0.0014 ft/s/pulse	0.00056 ft/s/pulse
Sample Rate	256 Hz	256 Hz
Gyro		
Bias	16.5°/h	2°/h
Scale-Factor Error	229 ppm	28 ppm
3-dB Bandwidth	50 Hz	50 Hz
g-Sensitive Drift	8.25°/h/g	1°/h/g
System		
Level Indication	98 μrad	25 μrad

The critical items in this specification are the accelerometer quantization, the bandwidth over which data must be accurate, and the data rates at which the motion sensor must provide accurate information. If the antenna could be vibration isolated from the aircraft, say at 20 Hz, then the data bandwidth requirements would be halved—a strongly recommended approach for an antenna-mounted motion sensor.

If a high-quality motion sensor cannot be mounted directly on the antenna, an alternate approach is possible. A low-performance wide-bandwidth motion sensor can be mounted directly on the hard-mounted

antenna and used in a master/slave configuration with a high-quality IMU mounted approximately 3 feet away. Basically, the antenna mounted system measures wide-bandwidth motions and the master measures low-frequency motions. The master/slave implementation has been studied in detail in Volume III and the requirements on the slave system and assumptions on the master are given in Table 2-5. This specification is for the EAR nominal SAR resolution. In Volume III the resolution achievable in the growth mode is evaluated using this system. The main result is that in the growth mode, adequate performance using this system at long range and low speed can only be achieved if the squint angle is approximately doubled.

In addition, a motion sensor to the antenna requires additional software to mechanize the master/slave filter and to mechanize the attitude and velocity update algorithms. The latter operations would be imbedded in the high-speed (256 Hz) motion-compensation calculations and would be expected to require a significant increase in the number of operations per second. Storage would also be affected.

The AFAL master/slave studies conducted in conjunction with this program used a 12-state Kalman filter with an iteration rate of once per second. No attempt at detailed suboptimal design was attempted; therefore, the additional computational requirements listed in Volume III should be viewed as the maximum.

Table 2-5. Master/slave system specification (nominal resolution).

Specification (1σ)	
Master System	
Level Indication	100 μrad
Azimuth Indication	600 μrad
Accelerometer Bias	50 μg
Accelerometer Scale-Factor Error	50 ppm
Slave System	
Accelerometer	
Bias	189 μg
Scale-Factor Error	85 ppm
3-dB Bandwidth	50 Hz
Quantization	0.0014 ft/s/pulse
Sample Rate	256 Hz
Gyro	
Bias	10°/h
Scale Factor	200 ppm
3-dB Bandwidth	50 Hz
g-Sensitive Drift	5°/h/g

SECTION 3

AVAILABLE SYSTEMS

CSDL conducted a survey of available components and systems in terms of their performance, reliability, and cost, for use as a slave system. In every instance, accelerometer performance and quantization for the systems is completely inadequate, data rates are too low and, in most cases, the slave system would be isolated from the antenna by vibration isolators. The latter point simply reflects that these systems were designed for navigation rather than as wide-bandwidth motion sensors. Further details of the systems considered are given in Appendix B of Volume III of the Final Report on this task. Table 3-1 gives the performance deficiencies of each system as presently identified. Several of the systems have gyro performance which is "too good"; this is not noted as a deficiency in performance, but is obviously reflected in the excessive cost of the particular system.

Table 3-1. Slave system survey.

Characteristic	Requirement	Lear Siegler P 5152A	Lear Siegler 2094A	Timex IG 16	Northrup GIG6	Honeywell H-478	Honeywell ATIGS	Raytheon LCP III	Autonetics Micron
Accelerometer Bias	189 μg	N	N	N	N	N	A	N	A
Accelerometer S.F. Error	85 ppm			N	N	N	N	N	A
Bandwidth	50Hz			N	N	A			
Quantization	0.0014 fps/pule	N	N	N	N	N	N	N	N
Sample Rate	256 Hz	A	A	N	N				N
Gyro Bias	10°/hr	A	A	A	N	A	A	A	A
Gyro S.F. Error	200 ppm			N	N	N	A		
Bandwidth	50Hz					A			
g Sensitive Drift	5°/hr/g	A	A			A			
Mounting Isolator	>50 Hz	A	A		A	A		A	N
Cold Start	Yes	A	A	A	A	A		A	A
Cost	<$35K	A	A			A	A	A	A
NOTES:		Includes Computer No Radiation hardening Gyro quantization too large.	Radiation hardening? Gyro Quantization too large	No Accelerometers in system Radiation hardening? Gyro Input rate too small	Limited production No Accelerometers in system Radiation hardening? Only 2 gyros	Limited Production	No production history Includes computer	No Production history Gimbal platform	No Production history

A = acceptable
N = not acceptable
Blank indicates information not available

SECTION 4

MODIFICATIONS TO EXISTING SYSTEMS

The identification of the deficiencies of available systems could lead to modification programs at the particular vendors' facilities. With the presently available information, CSDL has no way of assessing the technical feasibility or economic practicality of modifying these systems to perform as motion sensors. The critical issue is generally the mechanization of the accelerometer, its performance, its quantization, and the overall bandwidth and data rates of the system. Any modification program should address these issues immediately. In addition, the results of any modification program should be verified by independent laboratory testing.

Volume II details a CSDL conception of a design, fabrication, and test plan for a low-cost modular motion-sensing system. The initial phases of that program identify the type of investigation required to design and to verify adequate accelerometer performance. In addition, CSDL believes that the modular approach gives the Air Force a nonproprietary design which will allow low cost to be achieved by competitive bidding with no inherent sacrifice in reliability.

In either the modification to an existing system approach or the modular approach of Volume II, a parallel software development effort must be undertaken to analyze and implement a suboptimal master/slave filter, to develop and to implement the attitude and velocity algorithms, and to provide the necessary software control and initialization over the slave system. These efforts have no significant technical risk.

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